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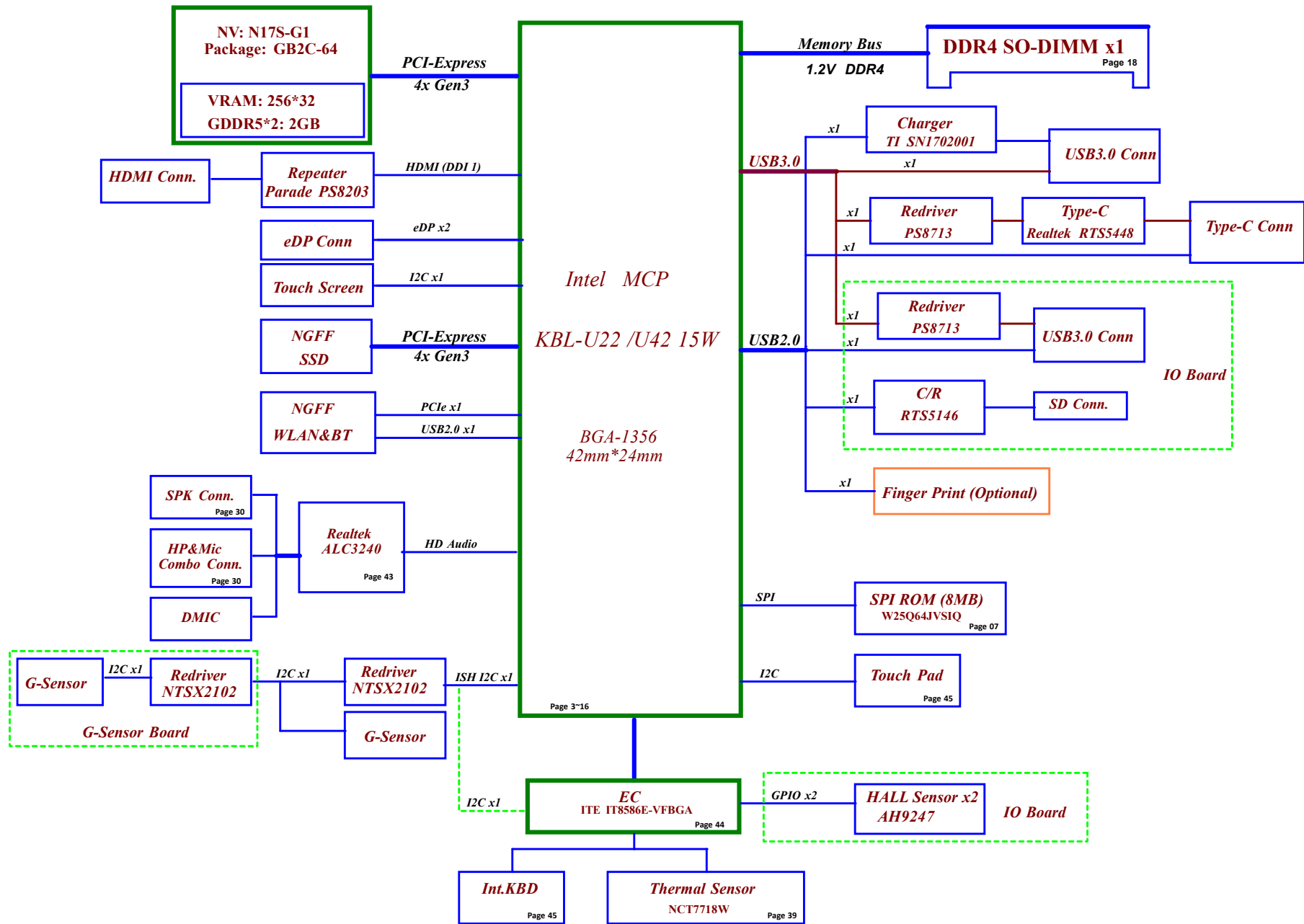
EYG10/ES430/ES530 MB Schematics Document

KBL-U22/U42 with DDR4 + Nvidia N16S-GTR/N17S-G1

2018-01

REV:1.0

| | | | | | | | | | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|------------------------------|--|---------------------------|--|---------------------------------------------------------------------------------------|--|---------|--|
| Security Classification | | LC Future Center Secret Data | | Title | |  | | | |
| Issued Date | | 2015/08/20 | | Deciphered Date | | 2016/08/20 | | | |
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| | | | | Custom | | EYG10 ES430 ES530 | | 1.0 | |
| Date: | | | | Tuesday, January 09, 2018 | | Sheet | | 1 of 60 | |



Voltage Rails (0 --> Means ON , X --> Means OFF)

| <div>Power Plane</div> <div>State</div> | | | | |
|-----------------------------------------|-------|--------------------------------------------------------|------------------------------|-------------------------------------------------------------------------------|
| | V20B+ | +3VALW +5VALW +3VALW_PCH +1.8VALW +1.0VALW | +1.2V +2.5V_DDR +VCCST | +5VS +3VS +VCCIO +VCCSTG +VCCSA +VCC_GT +CPU_CORE +0.6VS |
| S0 | 0 | 0 | 0 | 0 |
| S3 | 0 | 0 | 0 | X |
| S3 Battery only | 0 | 0 | 0 | X |
| S5 S4 AC Only | 0 | 0 | X | X |
| S5 S4 Battery only | 0 | X | X | X |
| S5 S4 AC & Battery don't exist | X | X | X | X |

SMBUS Control Table

| | SOURCE | BATT | Charger | DGPU | IT8586E | Memory Down | PCH | PMIC | SODIMM | Thermal Sensor | WLAN WiMAX |
|-----------------------------|--------------------|------|---------|---------------|--------------|----------------|-----------------|------|-----------|-------------------|---------------|
| EC_SMB_CK1 EC_SMB_DA1 | IT8586E +3VL_EC | V | V | X | V +3VL_EC | X | X | X | X | X | X |
| EC_SMB_CK2 EC_SMB_DA2 | IT8586E +3VS | X | X | V +3VG_AON | V +3VS | X | V +3VALW_PCH | X | X | V | X |
| EC_SMB_CK3 EC_SMB_DA3 | IT8586E +3VL_EC | X | X | X | V +3VL_EC | X | X | V | X | X | X |
| PCH_SMB_CLK PCH_SMB_DATA | PCH +3VALW_PCH | X | X | X | X | X | V +3VALW_PCH | X | V +3VS | X | V +3VS |

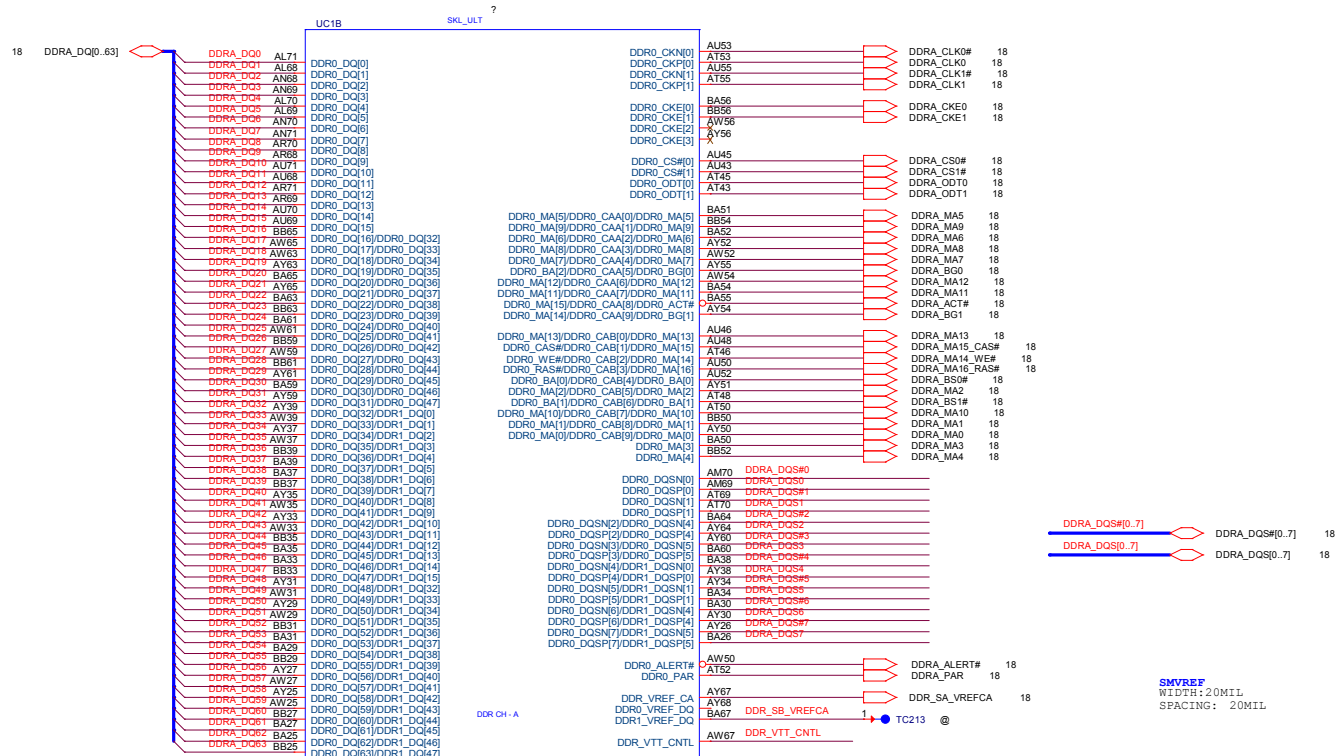
EC SMBus1 address EC SMBus2 address EC SMBus3 address PCH SM Bus address

| Device | Address | Device | Address | Device | Address | Device | Address |
|---------------|----------------|--------------------------|----------------|-------------|----------------|--------|----------|
| Smart Battery | need to update | Thermal Sensor(NCT7718W) | 1001_100xb | DDR4 SODIMM | need to update | Wlan | Reserved |
| Charger | 0001 0010 b | PCH | need to update | | | | |
| | | DGPU | need to update | | | | |

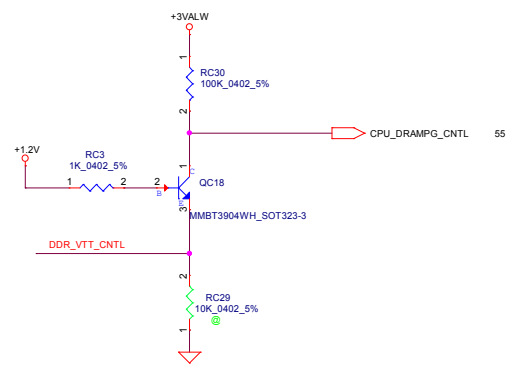
| STATE | SIGNAL | | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|----------------------|--------|--|---------|---------|---------|-------|-----|-----|-------|
| Full ON | | | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S3 (Suspend to RAM) | | | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | | | LOW | LOW | LOW | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | | | LOW | LOW | LOW | ON | OFF | OFF | OFF |
| | | | | | | | | | |


| HSIO PORT | | Function |
|-----------|------------|-------------------|
| USB3.0 | 1 | USB3.0 Conn Right |
| | 2 | USB3.0 Conn Left |
| | 3 | USB Type-C |
| | 4 | NC |
| | 5 | NC |
| | 6 | NC |
| USB2.0 | 1 | USB3.0 Conn Left |
| | 2 | USB Type-C |
| | 3 | USB3.0 Conn Right |
| | 4 | Finger Print |
| | 5 | Card reader |
| | 6 | Touch Panel |
| PCIE | 7 | Bluetooth |
| | 8 | Camera |
| | 9 | NC |
| | 10 | NC |
| | 1~4 X4 | DGPU |
| | 5 | WLAN |
| | 6 | NC |
| | 7~8 X2 | SSD-2 |
| | 9~12 X4 | SSD-1 |
| | | |

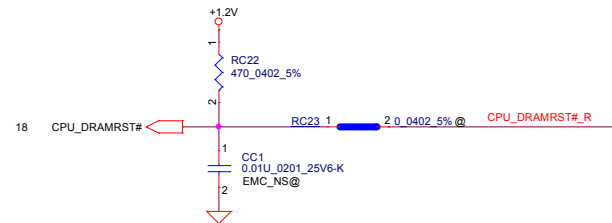
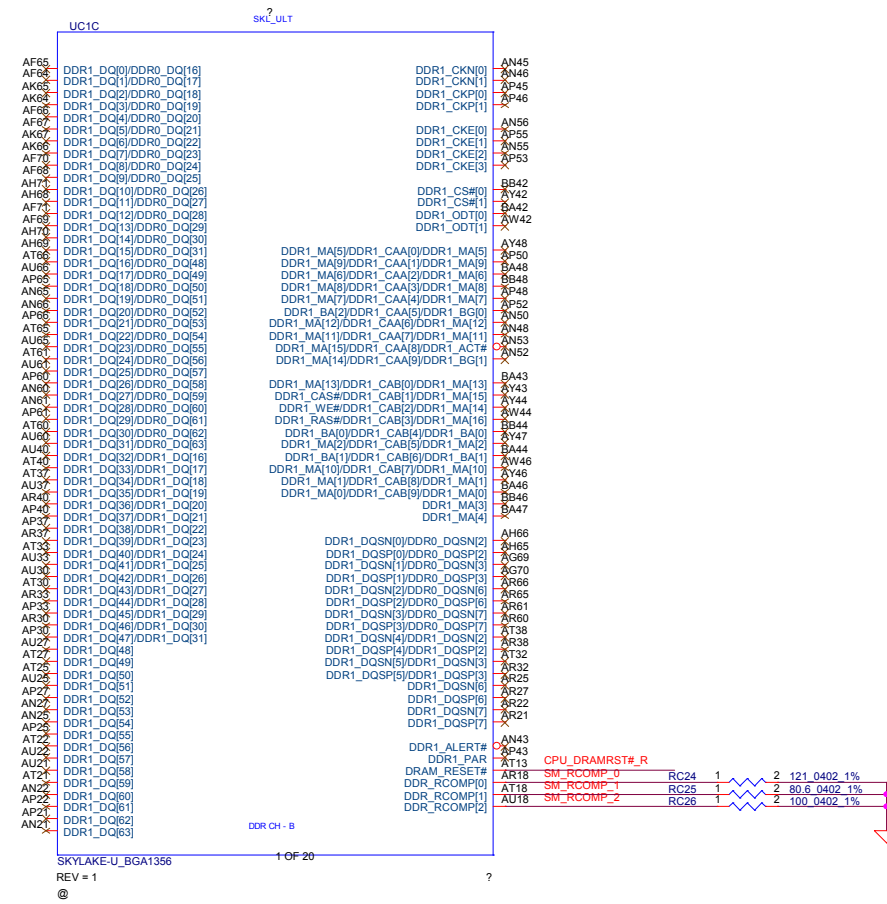
| BOM Structure | BTO Item |
|---------------|--------------------------|
| @ | Un-stuff |
| 14@ | For 14" part |
| 15@ | For 15" part |
| YOGA@ | For YOGA530 part |
| 530@ | For 530S part |
| | |
| | |
| CD@ | For C cost down |
| | |
| EMC@ | For EMC part |
| EMC_15@ | For EMC 15" part |
| EMC_NS@ | For EMC un-stuff part |
| EMC_PX@ | For EMC PX part |
| EMC_PXNS@ | For EMC PX nu-stuff part |
| | |
| | |
| ME@ | For ME part |
| | |
| | |
| OPT@ | For NV GPU part |
| OPTN16@ | For NV N16S-GTR GPU part |
| OPTN17@ | For NV N17S-G1 GPU part |
| | |
| | |
| | |
| TS@ | For touch screen part |
| TP@ | For Touch Pad Part |
| UMA@ | For UMA part |
| | |

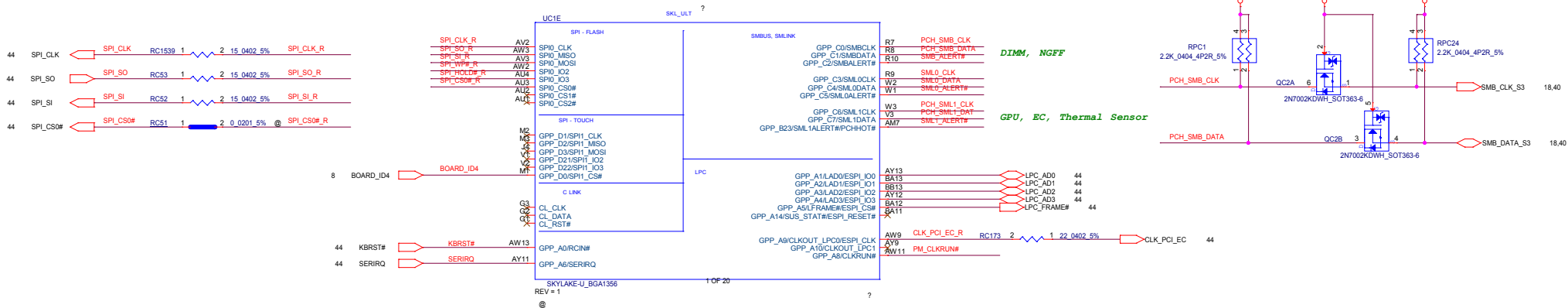


SKYLAKE-U_BGA1356
REV = 1



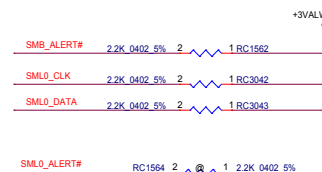
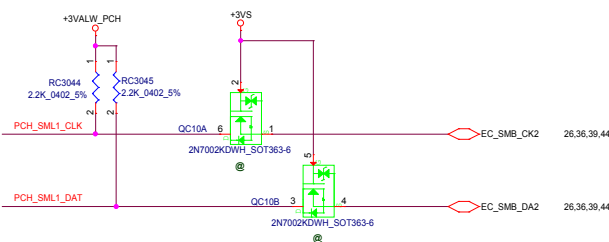
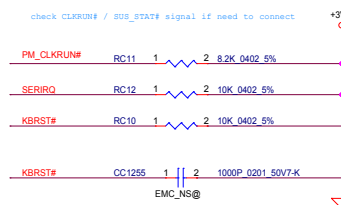
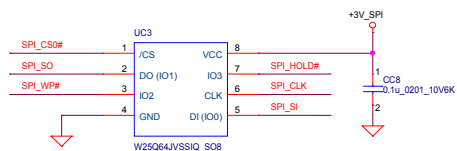
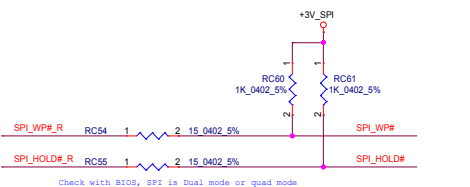
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| Size | | Document | | Number | | EYG10 ES430 ES530 | | | | |
| Custom | | | | | | | | | | |
| Date: | | | | Tuesday, January 09, 2018 | | | | Sheet 5 of 60 | | |





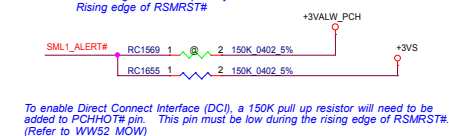
+3V_SPI

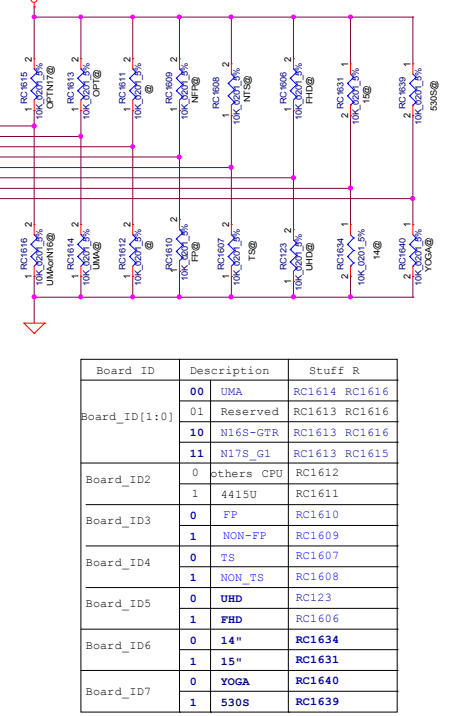
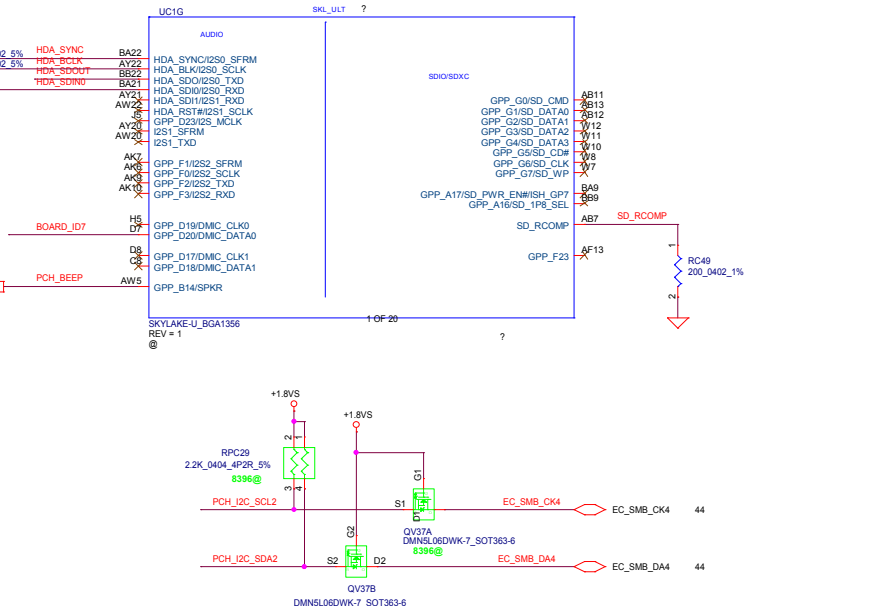
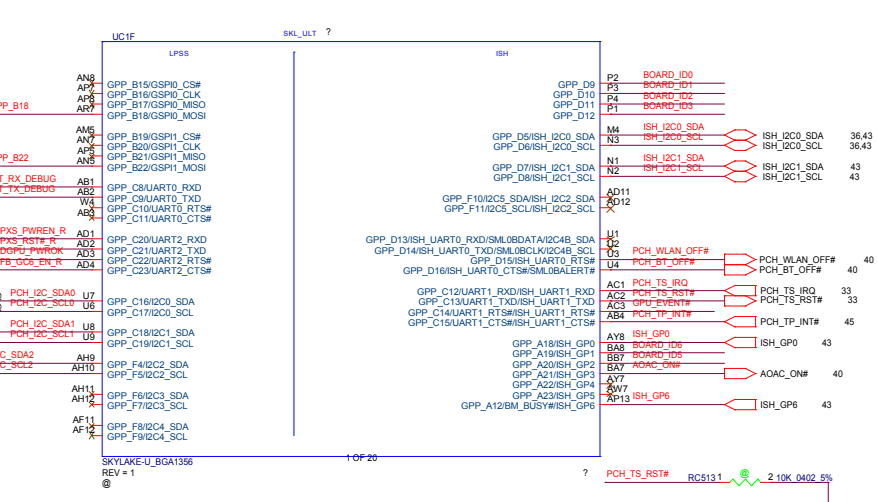
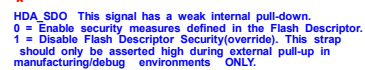
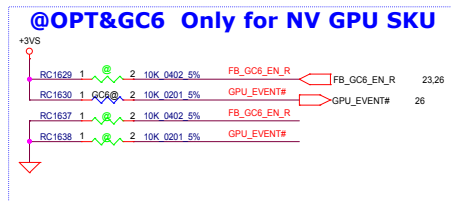
1. If support DS3, connect to +3VS and don't support EC mirror code;
2. If don't support DS3, connect to +3VALW_PCH and support EC mirror code.




This signal has a weak internal pull-down.
0 = LPC is selected for EC (Default)
1 = eSPI is selected for EC.


Notes:
1. The internal pull-down is disabled after RSMRST# de-asserts.
2. This signal is in the primary well
Rising edge of RSMRST#





| Board ID | Description | Stuff R |
|---------------|--------------|---------------|
| Board_ID[1:0] | 00 UMA | RC1614 RC1616 |
| | 01 Reserved | RC1613 RC1616 |
| | 10 N16S-GTR | RC1613 RC1616 |
| | 11 N16S_G1 | RC1613 RC1615 |
| Board_ID2 | 0 others CPU | RC1612 |
| | 1 4415U | RC1611 |
| Board_ID3 | 0 FP | RC1610 |
| | 1 NON-FP | RC1609 |
| Board_ID4 | 0 TS | RC1607 |
| | 1 NON TS | RC1608 |
| Board_ID5 | 0 UHD | RC123 |
| | 1 FHD | RC1606 |
| Board_ID6 | 0 14H | RC1634 |
| | 1 15" | RC1631 |
| Board_ID7 | 0 YOGA | RC1640 |
| | 1 530S | RC1639 |

| | | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------------------------|------------|--------------------------------------------------------------------------------------------------------------------|--|
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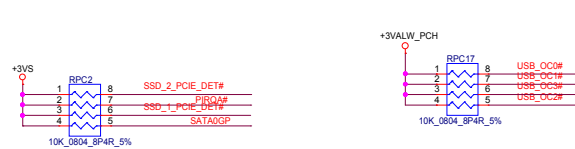
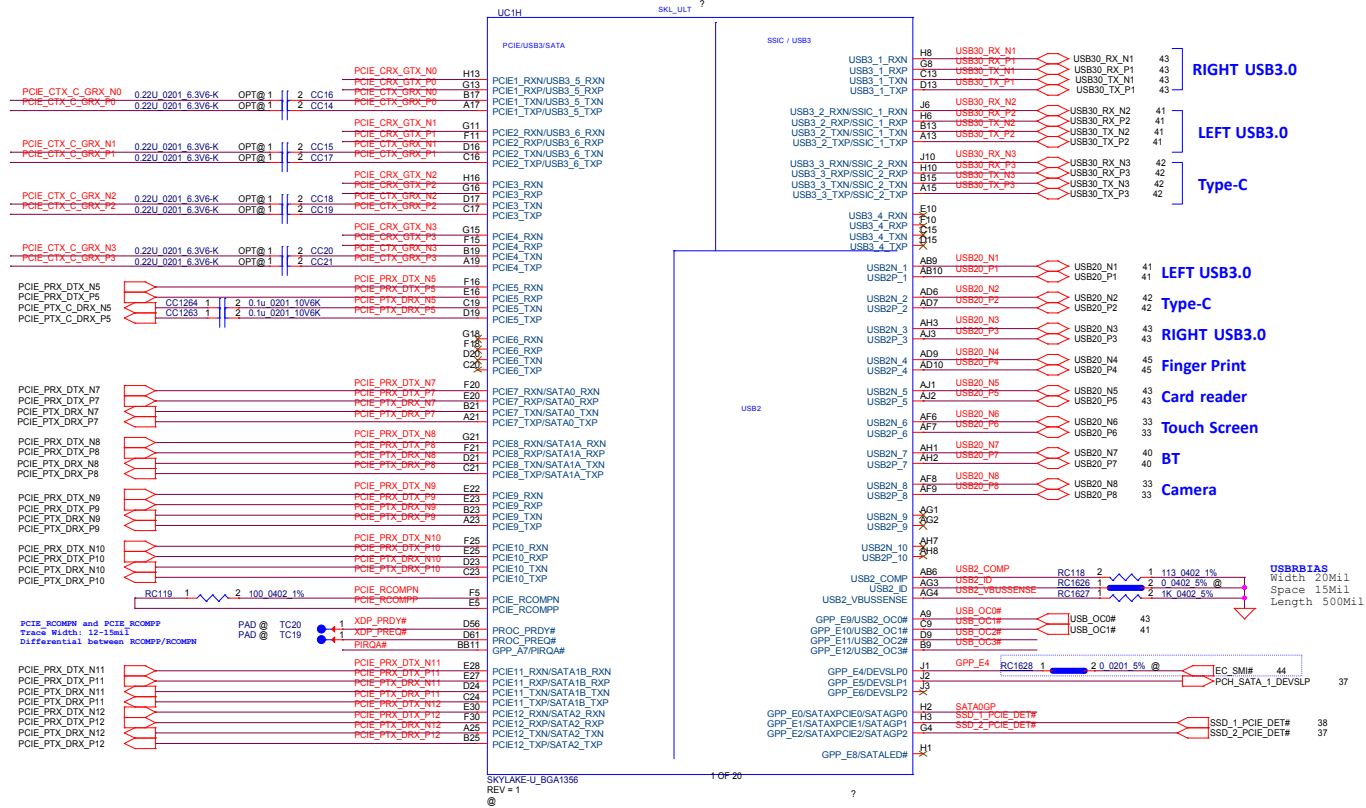
20 PCIE_CRX_GTX_N0.3] 
20 PCIE_CRX_GTX_P0.3] 
20 PCIE_CTX_C_GRX_N0.3] 
20 PCIE_CTX_C_GRX_P0.3] 

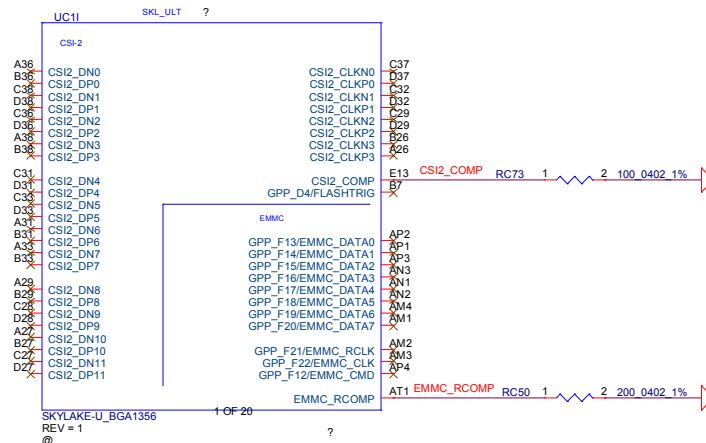
DGPU

WLAN

SSD 1

SSD 2

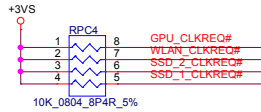




@DIS For NV GPU SKU

PCIE CLK0 DGPU

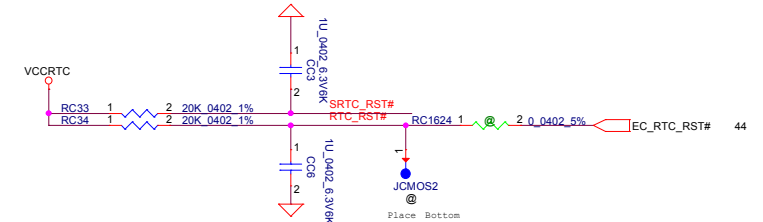
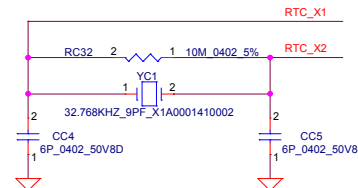
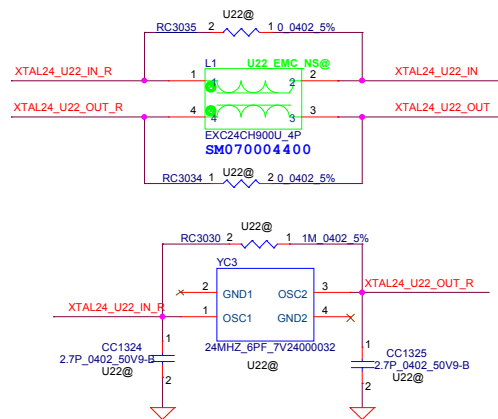
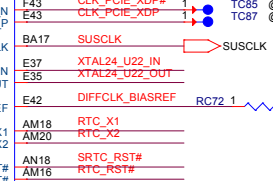
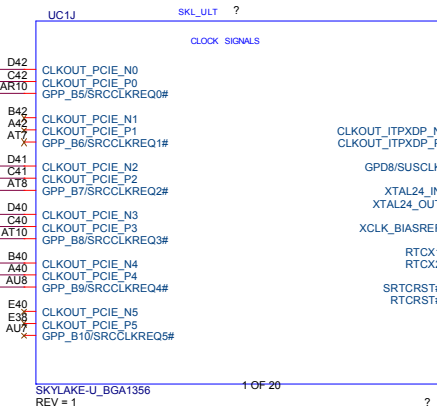
20 CLK_PCIE_GPU#
20 CLK_PCIE_GPU#
20 GPU_CLKREQ#



WLAN

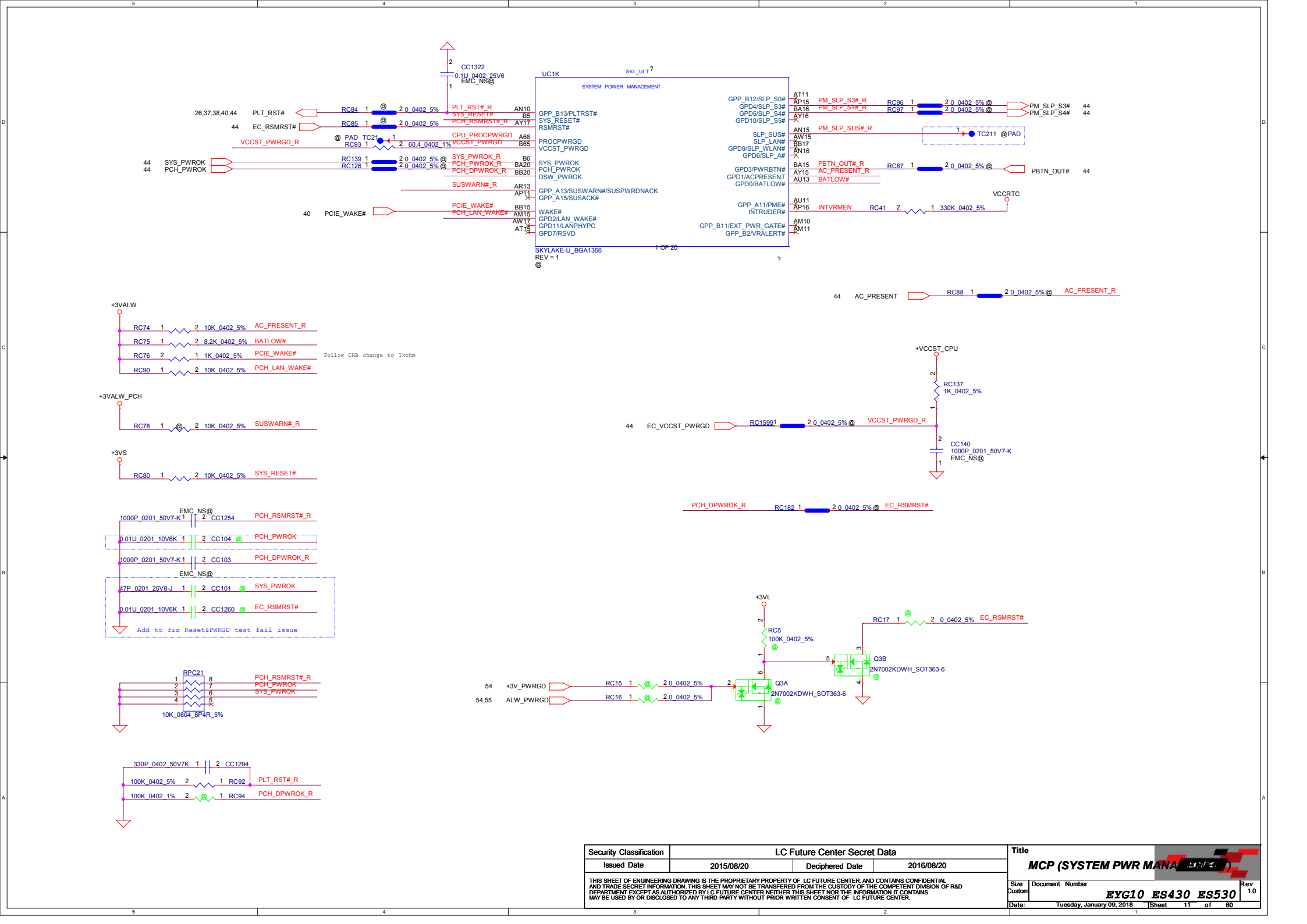
SSD-2

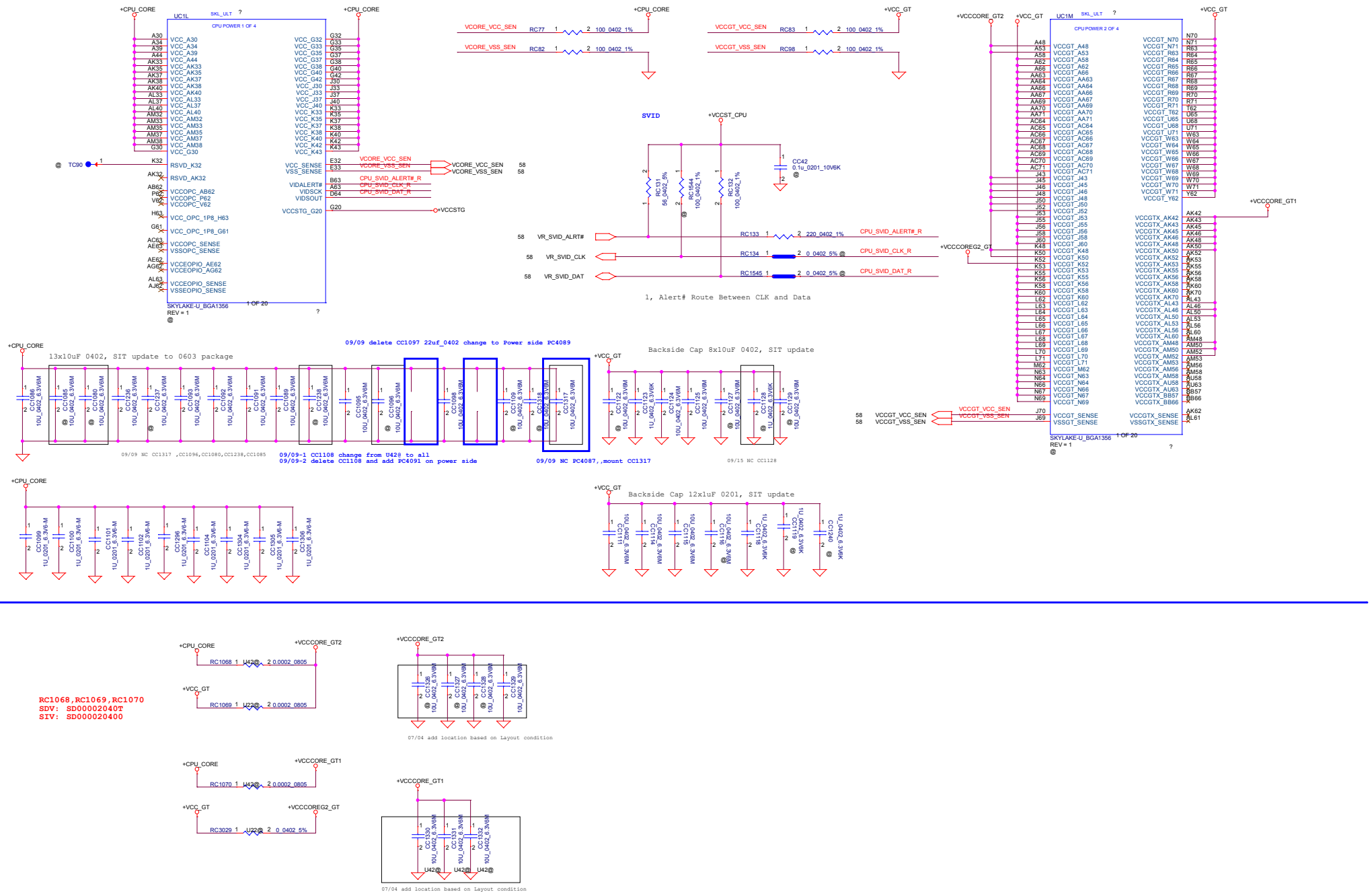
SSD-1

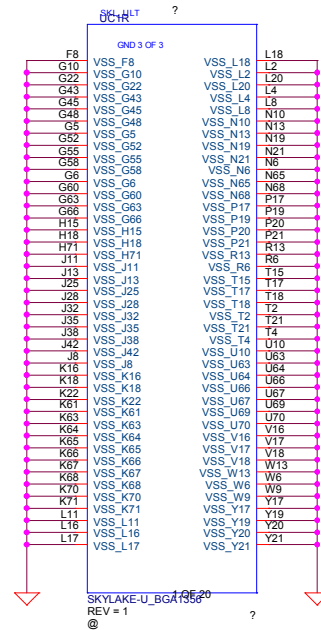
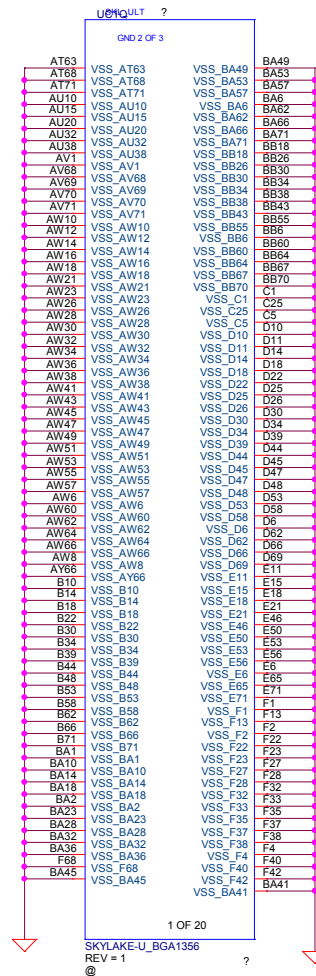
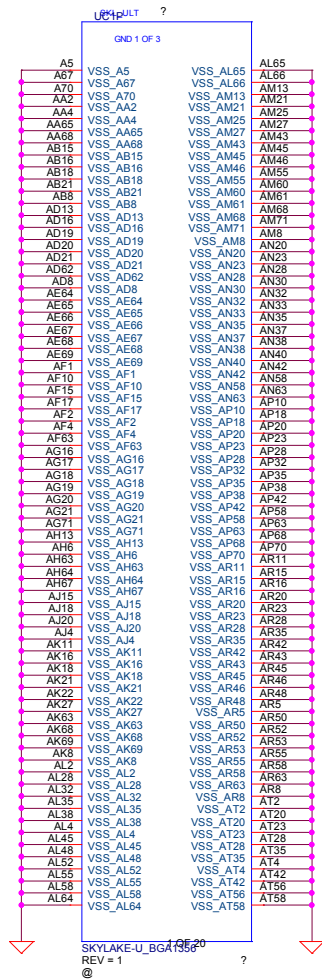


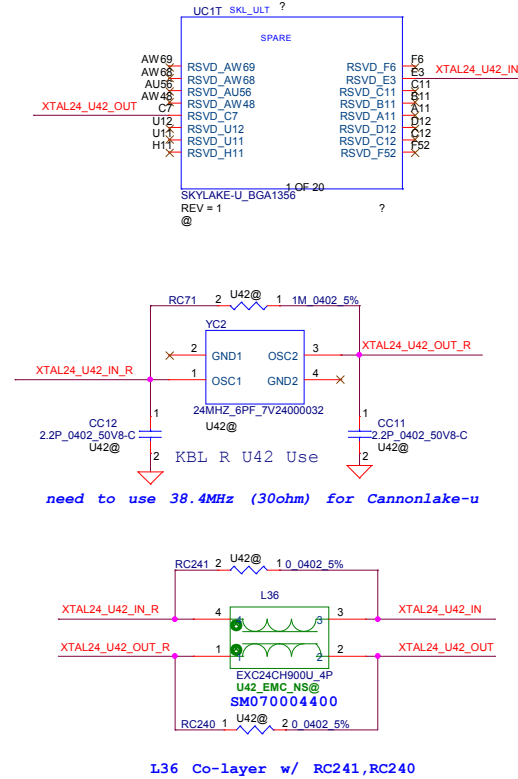
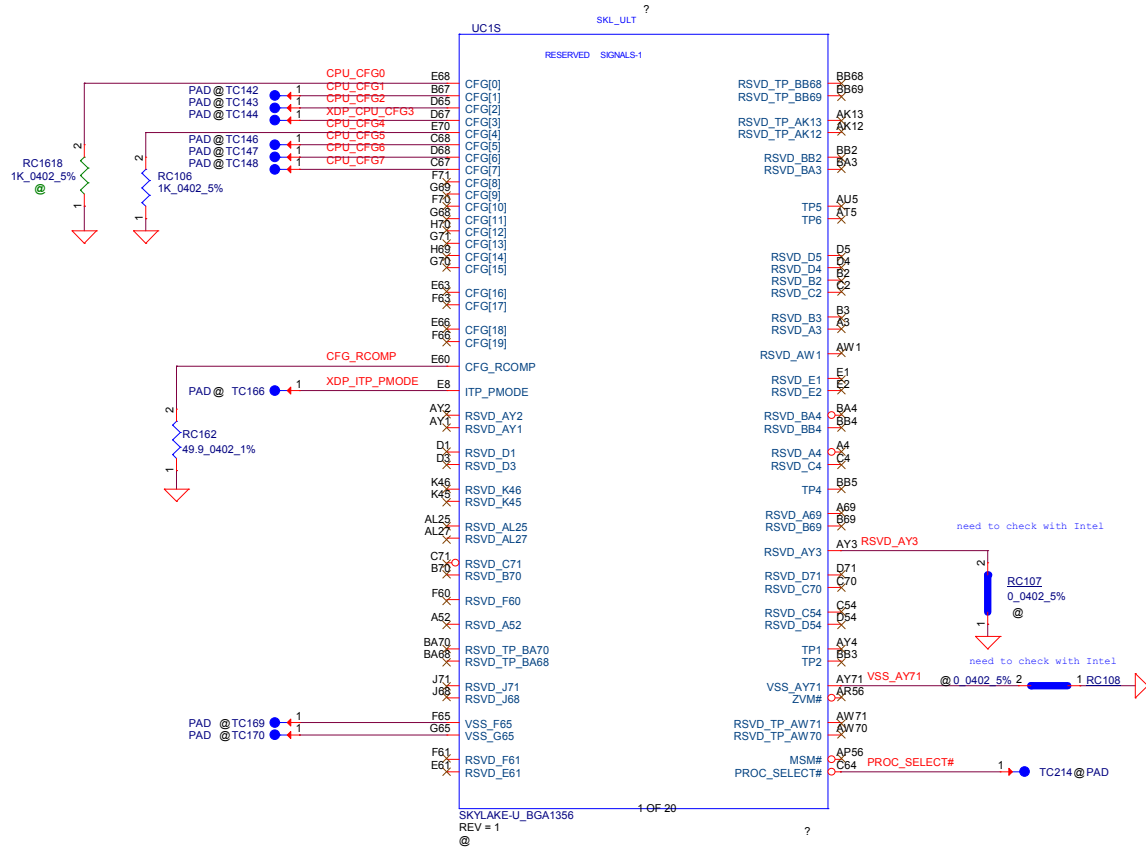
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| Title | | | |
|---------------------------|---------------------------|-------------------|----------|
| MCP (CSI2,EMMC,CLOCK) ICF | | | |
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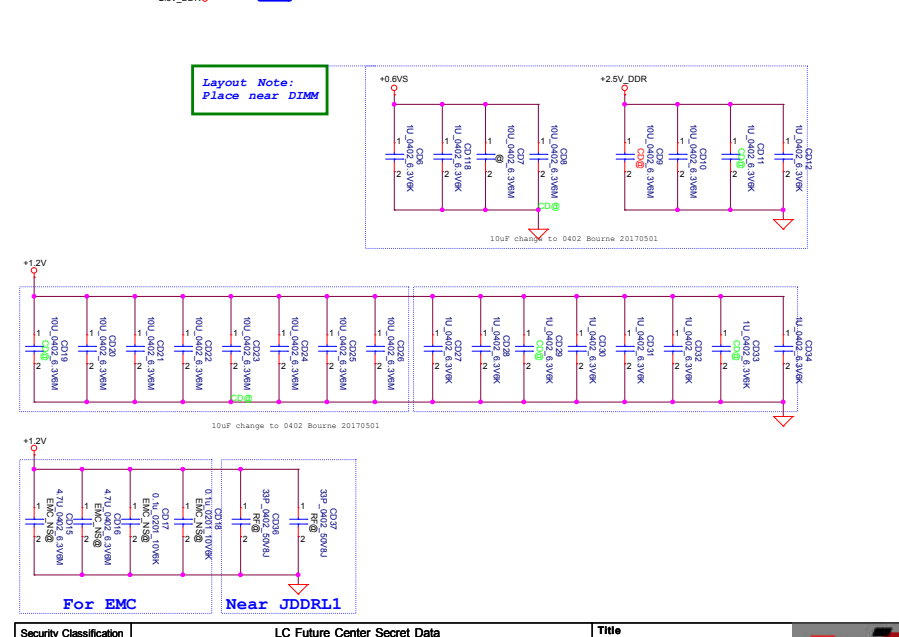
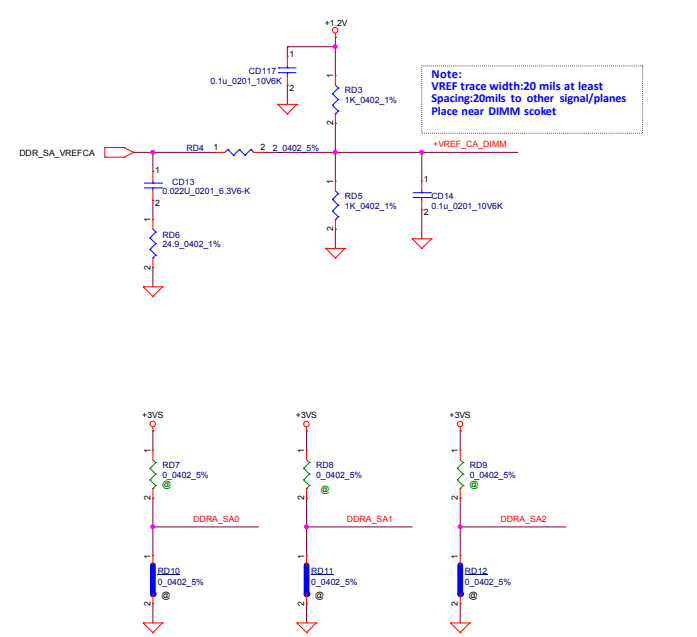
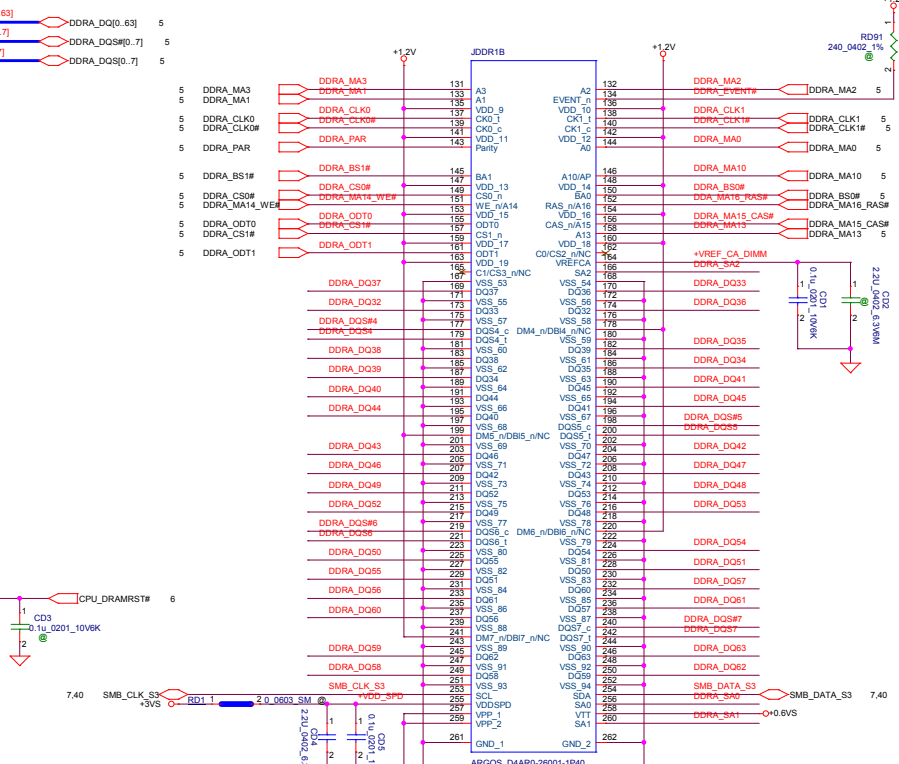
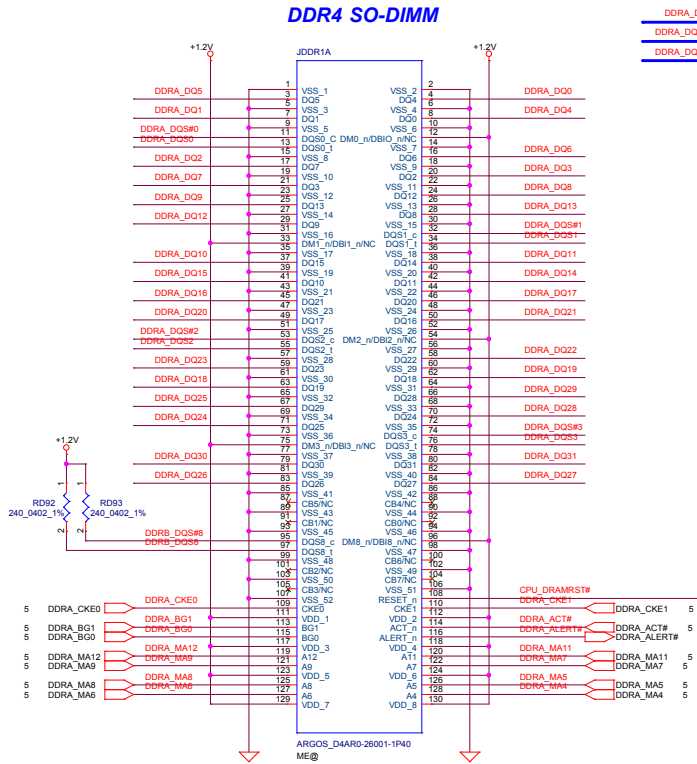


| Pin Name | Strap Description | Configuration | Default Value |
|----------|-----------------------------|------------------------------------------|---------------|
| CFG[4] | Display Port Presence strap | - 1 = eDP Disabled - 0 = eDP Enabled★ | 1 |

| | | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|------------------------------|--|----------------------|--|
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DDR4 SO-DIMM



SPD Address = A0

| | | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|------------------------------|------------|--------------|----------|
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| Date | Tuesday, January 09, 2018 | | | Sheet | 18 of 60 |

N16x GPIO

| GPIO | I/O | ACTIVE | Function Description |
|--------|-----|--------|--------------------------------------------------|
| GPIO0 | OUT | - | GPU Core VDD PWM control signal |
| GPIO1 | OUT | N/A | FB Enable for GC6 2.0 |
| GPIO2 | OUT | N/A | |
| GPIO3 | OUT | N/A | |
| GPIO4 | OUT | N/A | |
| GPIO5 | OUT | N/A | GPU power sequencing--3V3_MAIN_EN |
| GPIO6 | IN | - | GPU wake signal for GC6 2.0 |
| GPIO7 | OUT | N/A | |
| GPIO8 | I/O | - | System side PCIe reset Monitor |
| GPIO9 | I/O | N/A | 2.2K Pull-up |
| GPIO10 | OUT | | FBVREF_ALTV for GDDR5 |
| GPIO11 | OUT | - | |
| GPIO12 | IN | | AC Power Detect Input (10K pull High) |
| GPIO13 | OUT | - | Phase Shedding |
| GPIO14 | IN | N/A | |
| GPIO15 | IN | N/A | |
| GPIO16 | | N/A | |
| GPIO17 | IN | N/A | |
| GPIO18 | IN | N/A | |
| GPIO19 | IN | N/A | |
| GPIO20 | | N/A | |
| GPIO21 | OUT | | GPU PCIe self-reset control |
| OVERT | OUT | | Active Low Thermal Catastrophic Over Temperature |

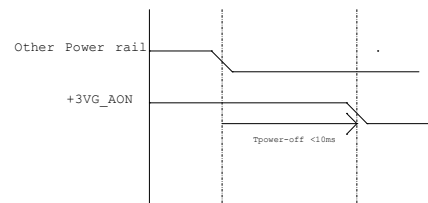
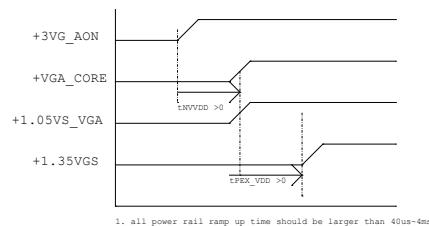
Performance Mode P0 TDP and EDP-Continuous current (GDDR5)

| | GPU | Mem | Min Core Clk | NVVDD | | | FBVDD (1.35V) | | FBVDDQ (GPU+Mem) (1.35V) | | (1.05V) (6) | | Other (3.3V) | |
|----------|-----|-----|--------------|-------|------|-----|---------------|-----|--------------------------|-----|-------------|-----|--------------|-----|
| Products | (W) | (W) | (MHz) | (V) | (A) | (W) | (A) | (W) | (A) | (W) | (mA) | (W) | (mA) | (W) |
| N16S-GMR | 16 | 1.6 | 849 | TBD | 19 | TBD | 2 | TBD | 4.2 | TBD | 800 | TBD | 60 | TBD |
| N16S-GTR | 18 | 1.7 | 967 | | 26.5 | | 2 | | 4.2 | | 800 | | 60 | |

N16x Multi-level Straps

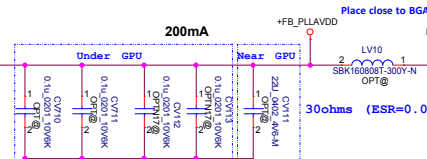
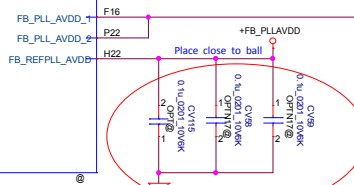
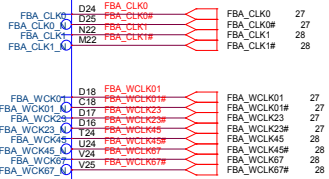
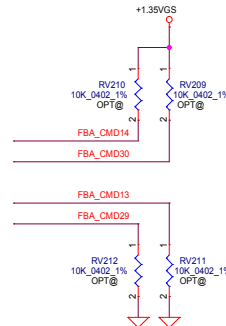
| Physical Strapping pin | Power Rail | Logical Strapping Bit3 | Logical Strapping Bit2 | Logical Strapping Bit1 | Logical Strapping Bit0 |
|------------------------|------------|-------------------------------------------------------------------------|------------------------|------------------------|------------------------|
| ROM_SCLK | +3VGS | SOR3_EXPOSED | SOR2_EXPOSED | SOR1_EXPOSED | SOR0_EXPOSED |
| ROM_SI | +3VGS | RAM_CFG[3] | RAM_CFG[2] | RAM_CFG[1] | RAM_CFG[0] |
| ROM_SO | +3VGS | DEVID_SEL | PCIE_CFG | SMB_ALT_ADDR | VGA_DEVICE |
| STRAP0 | +3VGS | Reserved(keep pull-up and pull-down footprint and stuff 50Kohm pull-up) | | | |
| STRAP1 | +3VGS | | | | |
| STRAP2 | +3VGS | Reserved(keep pull-up and pull-down footprint and not stuff by default) | | | |
| STRAP3 | +3VGS | | | | |
| STRAP4 | +3VGS | | | | |

N15V-GM Power Sequence



| Security Classification | LC Future Center Secret Data | | | Title | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----------------|------------|----------------|---------------------------|
| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | VGA Notes List | |
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| | | | | | Rev |
| | | | | Date: | Tuesday, January 05, 2018 |
| | | | | Sheet | 19 of 60 |

27.28 FBA_D[0..63]
27.28 FBA_CMD[31..0]
27.28 FBA_EDC[7..0]
27.28 FBA_DBI[7..0]

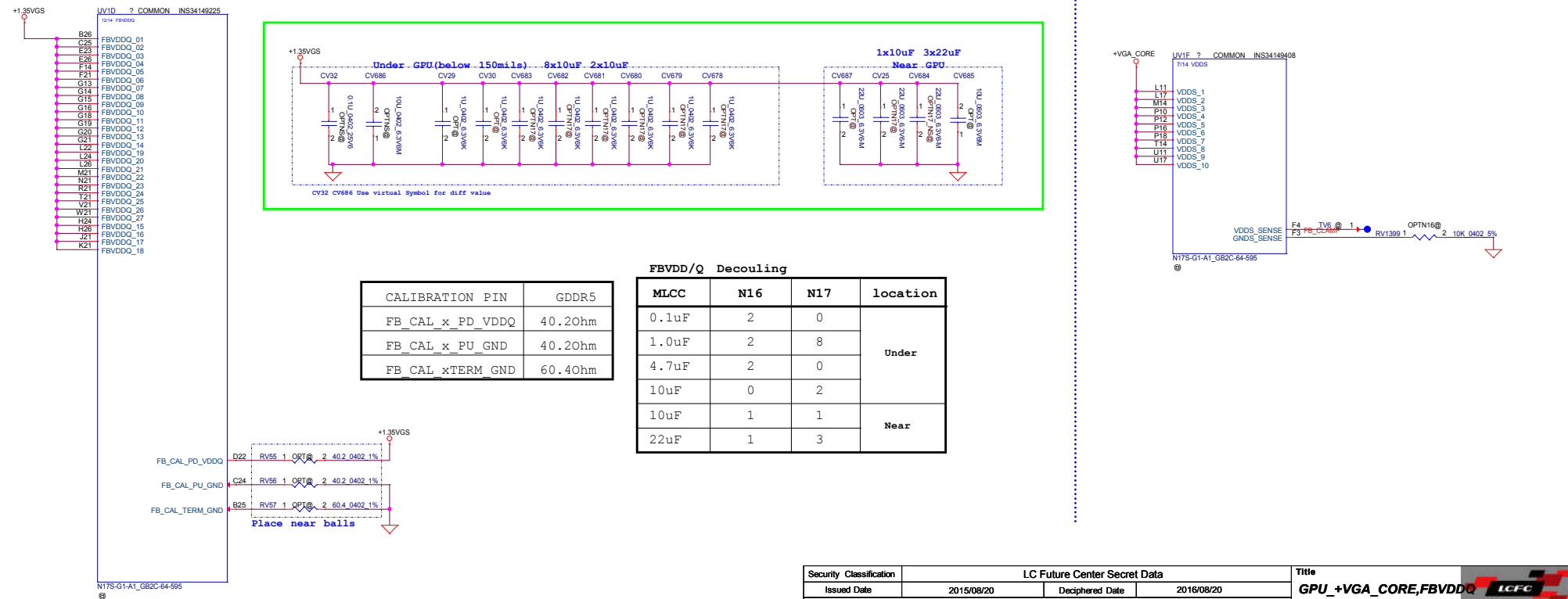
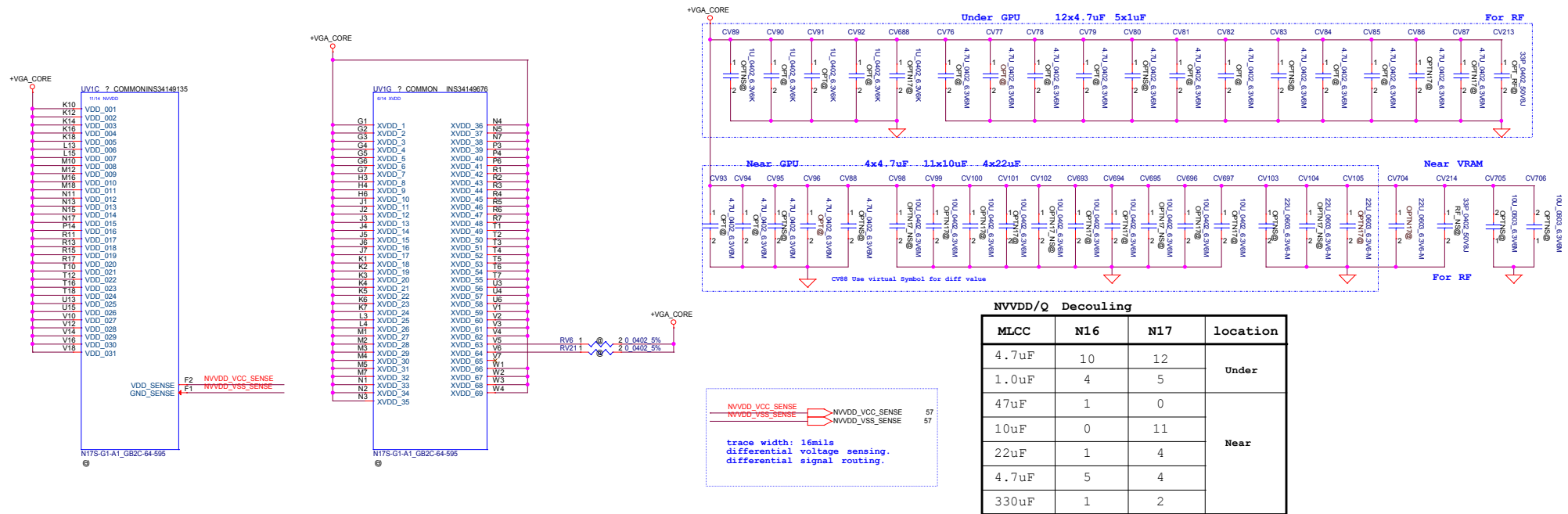


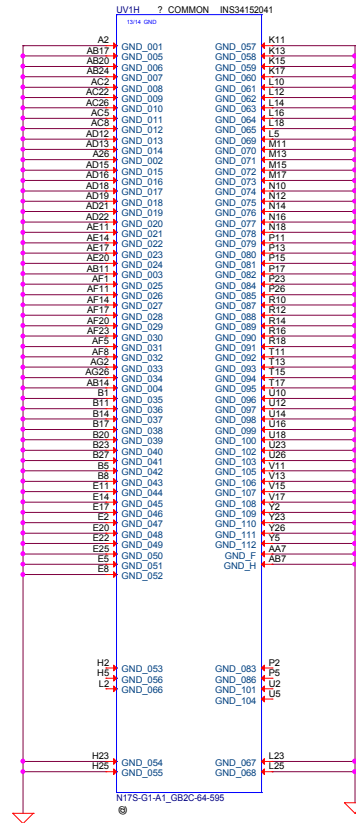
FB_PLL/Q Decoupling

| MLCC | N16 | N17 | location |
|-------|-----|-----|----------|
| 0.1uF | 2 | 4 | Under |
| 22uF | 1 | 1 | Near |

| | | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----------------|
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| Issued Date | 2015/08/20 | Deciphered Date |
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|-------------------|---------------------------|---------------------------------------------------------------------------------------|----------|
| Title | |  | |
| GPU_MEM Interface | | | |
| Size | Document Number | Rev | |
| C | EYG10 ES430 ES530 | 1.0 | |
| Date | Tuesday, January 08, 2018 | Sheet | 21 of 60 |



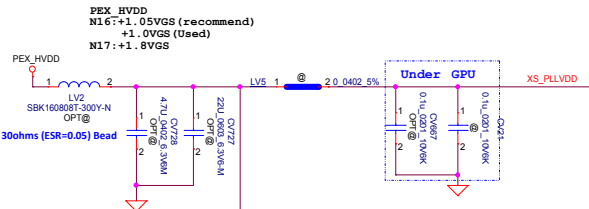
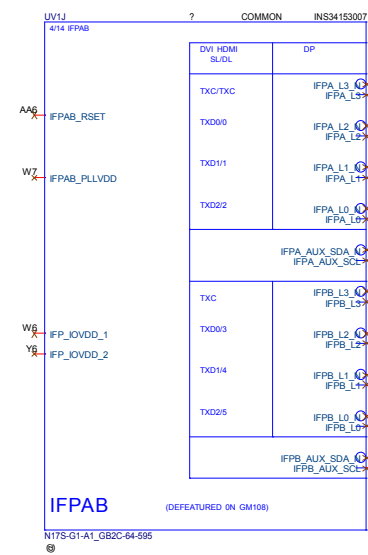
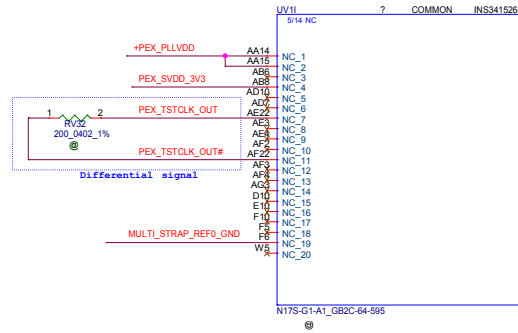
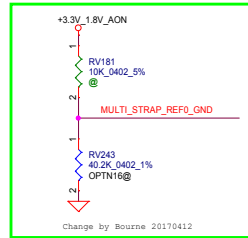
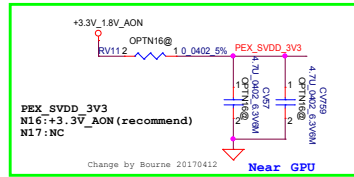
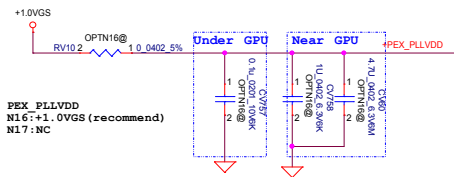


PEX_PLLVDD/Q Decoupling

| MLCC | N16 | N17 | location |
|-------|-----|-----|----------|
| 1.0uF | 1 | NA | Under |
| 1uF | 1 | NA | Near |
| 4.7uF | 1 | NA | |

PEX_SVDD/Q Decoupling

| MLCC | N16 | N17 | location |
|-------|-----|-----|----------|
| 4.7uF | 2 | NA | Near |



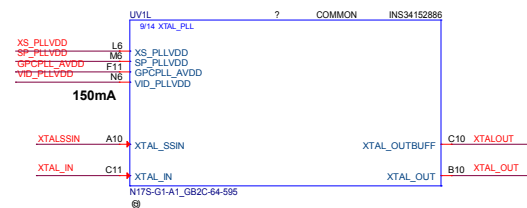
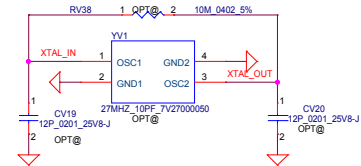
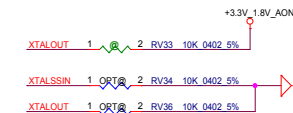
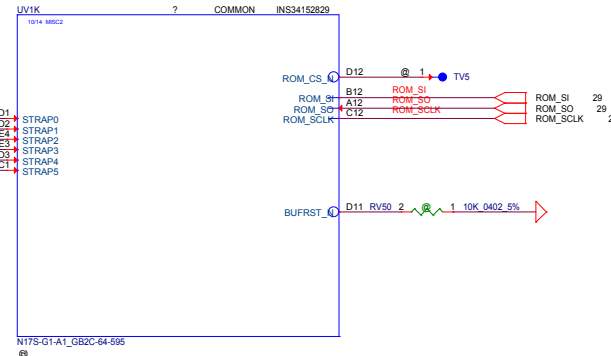
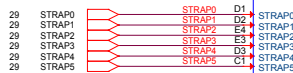
| MLCC | N16 | N17 | location |
|-------|-----|-----|----------|
| 0.1uF | 1 | 1 | Under |
| 22uF | 1 | 0 | Near |

SP_PLLVDD & VID_PLLVDD/Q Decoupling

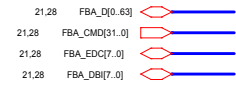
| MLCC | N16 | N17 | location |
|-------|-----|-----|----------|
| 0.1uF | 2 | 2 | Under |
| 10uF | 1 | 0 | Near |
| 47uF | 1 | 0 | |

GPCPLL_AVDD/Q Decoupling

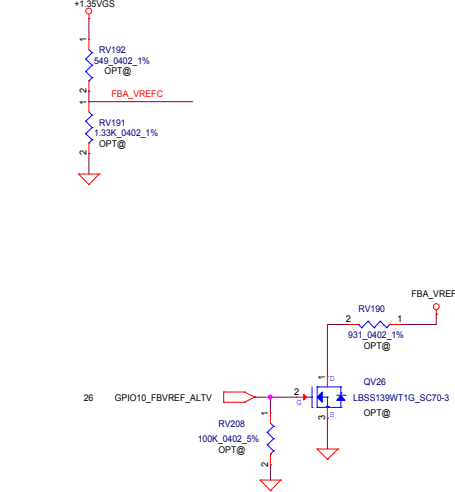
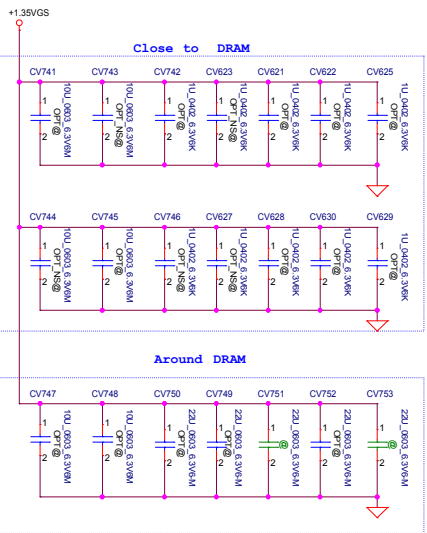
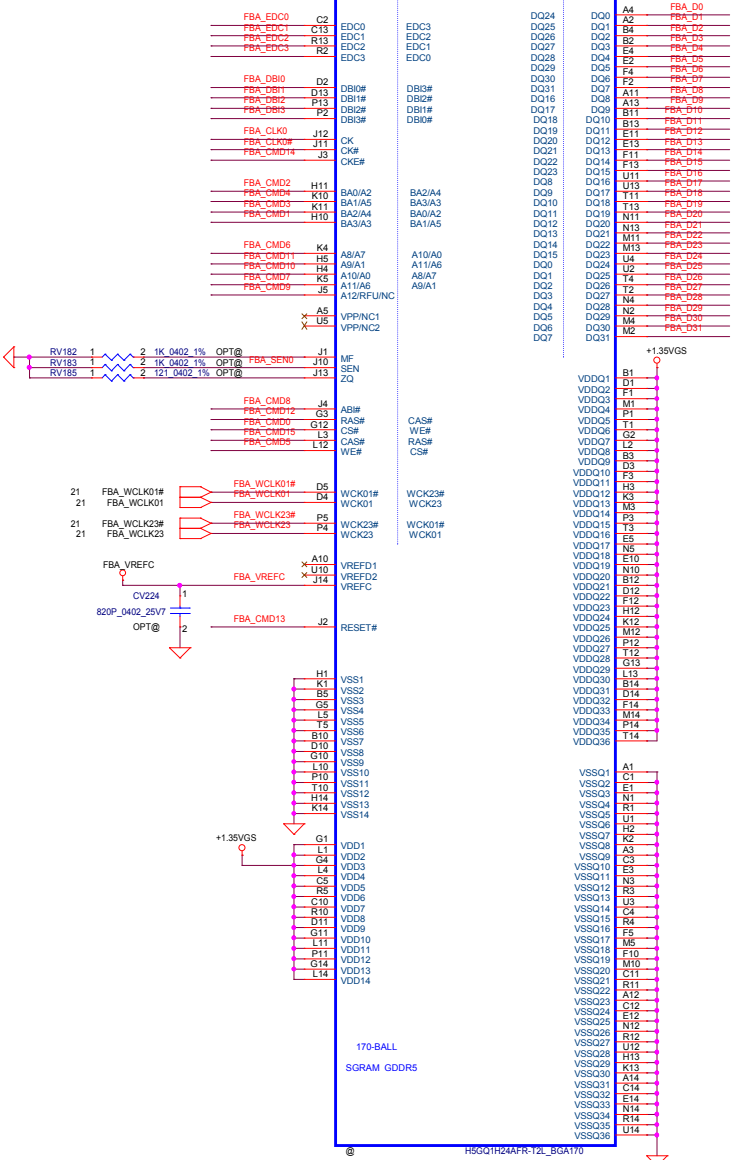
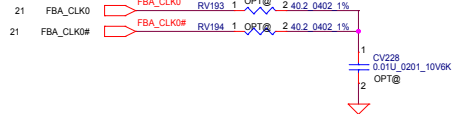
| MLCC | N16 | N17 | location |
|-------|-----|-----|----------|
| 0.1uF | NA | 1 | Under |
| 4.7uF | NA | 1 | Near |
| 22uF | NA | 1 | |

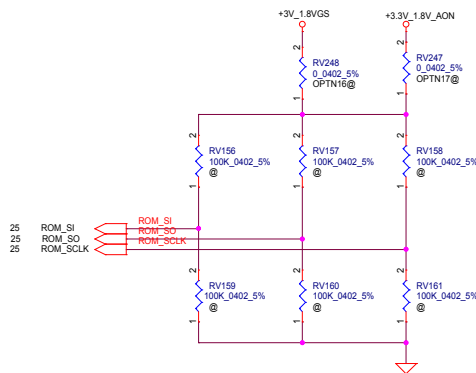
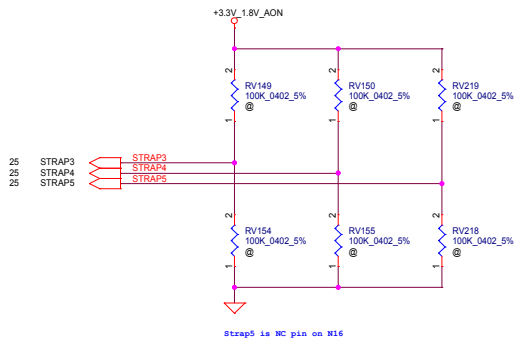
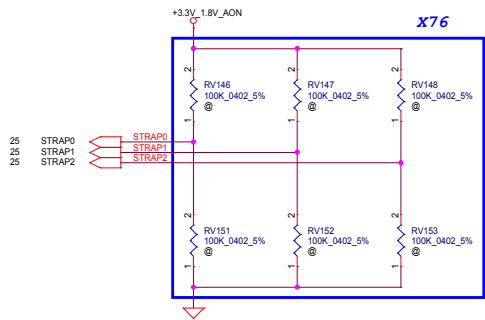


Lower 32 bits



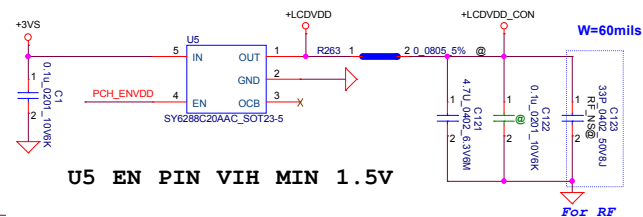
MF=0 No Mirror



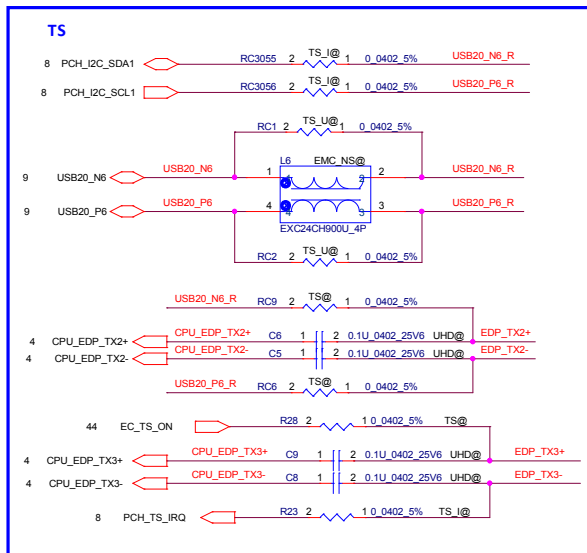
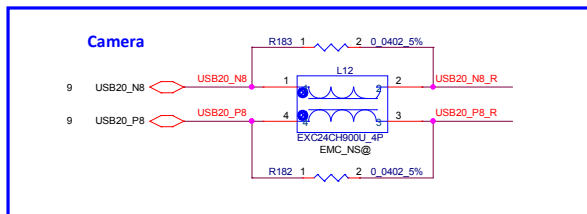
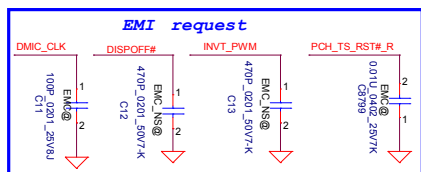
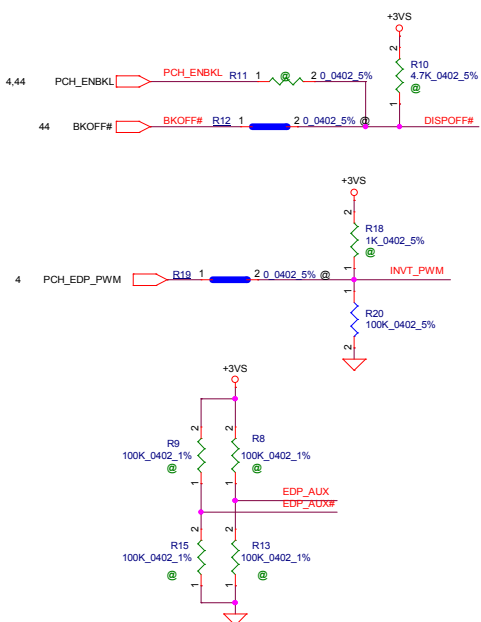
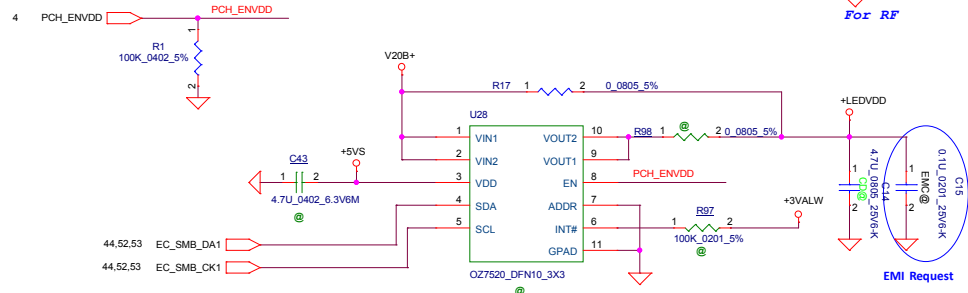


| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|--------------------------|------------|--------------------------------------------------------------------------------------|-------------------------|------------------------------|--|--|-------|-------------|------------|-----------------|------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|--|--|--------------------------------------------------------------------------------------|------|----------|--------|-----|--|--------|--|--------------------------|-----|--|-------|---------------------------|--|--|----------------|
| 5 | 4 | 3 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| D | | | | D | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| C | | | | C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| B | | | | B | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A | | | | A | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <table><tr><td>Security Classification</td><td colspan="3">LC Future Center Secret Data</td><td>Title</td></tr><tr><td>Issued Date</td><td>2015/08/20</td><td>Deciphered Date</td><td>2016/08/20</td><td>Blank</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td></td></tr><tr><td>Size</td><td>Document</td><td>Number</td><td colspan="2">Rev</td></tr><tr><td>Custom</td><td></td><td>EYG10 ES430 ES530</td><td colspan="2">1.0</td></tr><tr><td>Date:</td><td colspan="3">Tuesday, January 09, 2018</td><td>Sheet 32 of 60</td></tr></table> | | | | | Security Classification | LC Future Center Secret Data | | | Title | Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | Blank | THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER. | | | |  | Size | Document | Number | Rev | | Custom | | EYG10 ES430 ES530 | 1.0 | | Date: | Tuesday, January 09, 2018 | | | Sheet 32 of 60 |
| Security Classification | LC Future Center Secret Data | | | Title | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | Blank | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Size | Document | Number | Rev | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Custom | | EYG10 ES430 ES530 | 1.0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Date: | Tuesday, January 09, 2018 | | | Sheet 32 of 60 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | 4 | 3 | 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

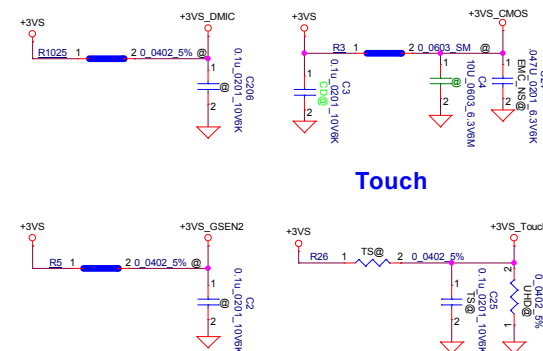
LCD POWER CIRCUIT



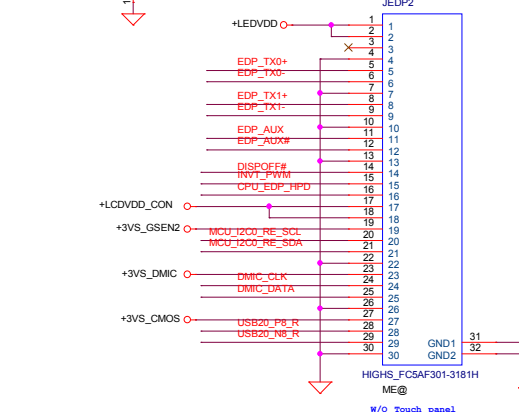
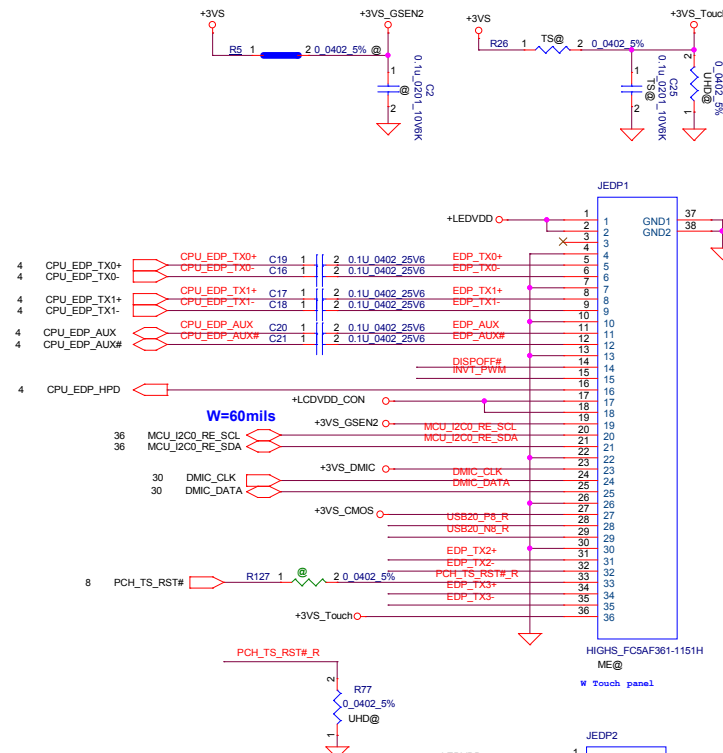
U5 EN PIN VIH MIN 1.5V



CMOS Camera



Touch

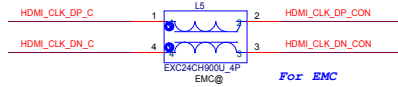
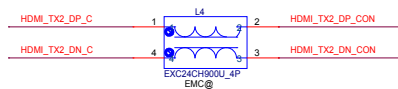
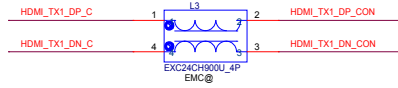
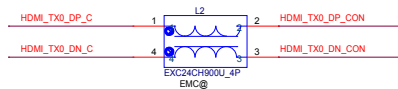
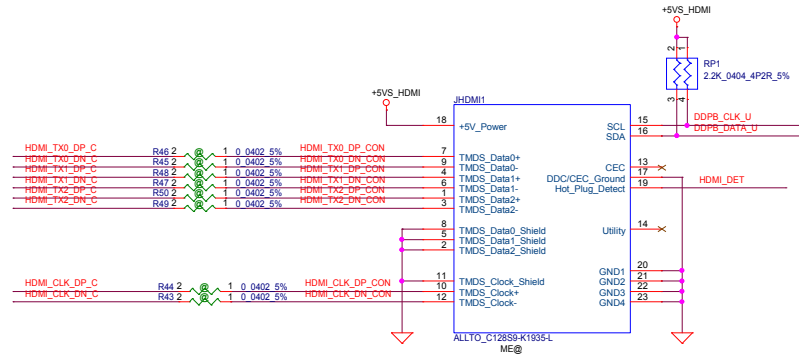
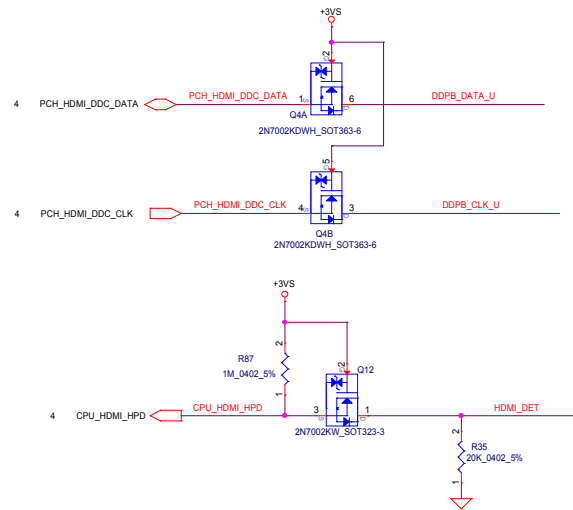
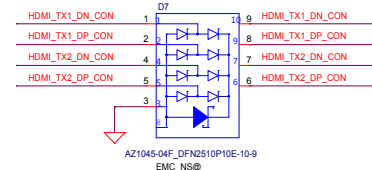
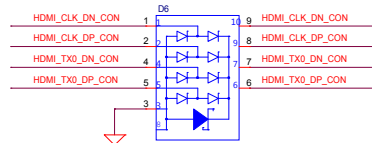
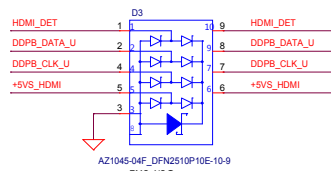
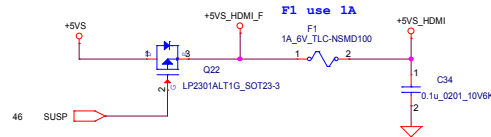
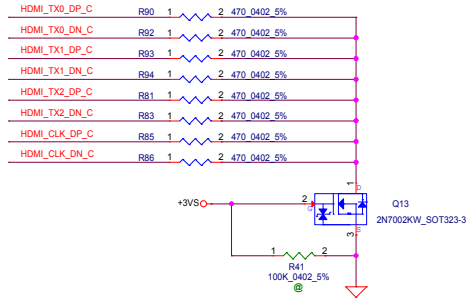


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|-------------|---------------------------|---------------------|----|---------------------------------------------------------------------------------------|---------|
| Title | | eDP/CAMERA/TS_CONN. | |  | |
| Size Custom | Document Number | EYG10 ES430 ES530 | | | Rev 1.0 |
| Date: | Tuesday, January 09, 2018 | Sheet | 33 | of | 60 |

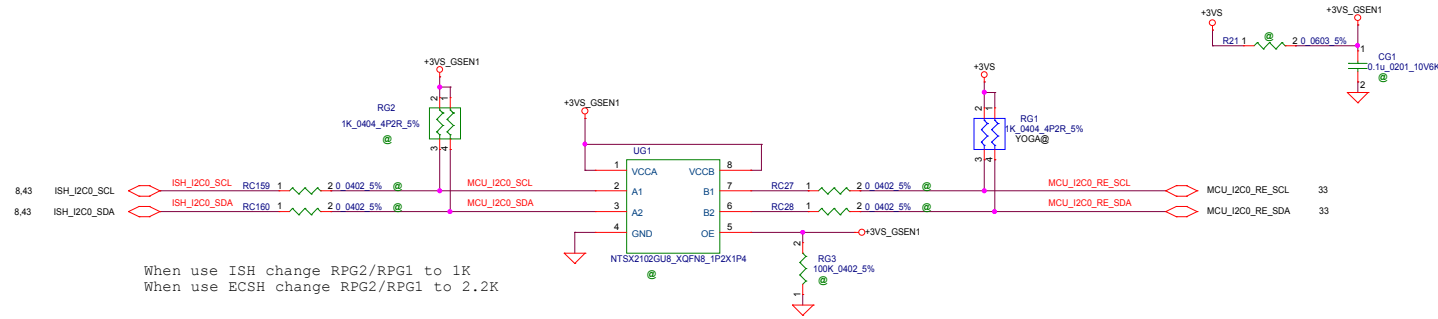
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|---|---------------|---------------|-----|---|---|-----------------|---------------|
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| 4 | CPU_HDMI_TXN2 | CPU_HDMI_TXN2 | C41 | 2 | 1 | 0.1u_0201_10V6K | HDMI_TX2_DN_C |
| 4 | CPU_HDMI_TXP1 | CPU_HDMI_TXP1 | C40 | 2 | 1 | 0.1u_0201_10V6K | HDMI_TX1_DP_C |
| 4 | CPU_HDMI_TXN1 | CPU_HDMI_TXN1 | C39 | 2 | 1 | 0.1u_0201_10V6K | HDMI_TX1_DN_C |
| 4 | CPU_HDMI_TXP0 | CPU_HDMI_TXP0 | C38 | 2 | 1 | 0.1u_0201_10V6K | HDMI_TX0_DP_C |
| 4 | CPU_HDMI_TXN0 | CPU_HDMI_TXN0 | C37 | 2 | 1 | 0.1u_0201_10V6K | HDMI_TX0_DN_C |
| 4 | CPU_HDMI_CLKP | CPU_HDMI_CLKP | C36 | 2 | 1 | 0.1u_0201_10V6K | HDMI_CLK_DP_C |
| 4 | CPU_HDMI_CLKN | CPU_HDMI_CLKN | C35 | 2 | 1 | 0.1u_0201_10V6K | HDMI_CLK_DN_C |



| | | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----------------|------------|-----------|---------------------------|
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| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | Size | Document Number |
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| | | | | Date: | Tuesday, January 08, 2018 |
| | | | | Sheet | 34 of 80 |

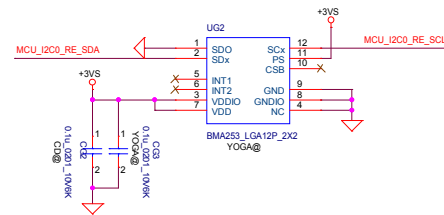
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| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | Blank | | |
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| | | | | | EYG10 ES430 ES530 | 1.0 |
| Date: Tuesday, January 09, 2018 | | | | Sheet | 35 | of 60 |

G-SENSOR

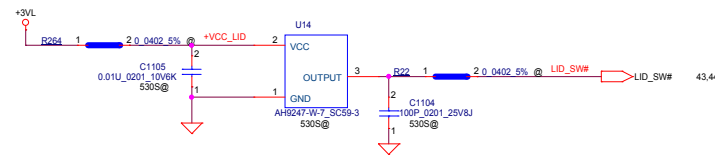


7.26.39.44 EC_SMB_CK2 RC3049 1 2 0.0402 5% @ MCU_I2C0_SCL
7.26.39.44 EC_SMB_D42 RC3050 1 2 0.0402 5% @ MCU_I2C0_SDA

ISH_I2C0_SCL RG4 1 2 0.0402 5% @ MCU_I2C0_RE_SCL
ISH_I2C0_SDA RG5 1 2 0.0402 5% @ MCU_I2C0_RE_SDA



LID switch

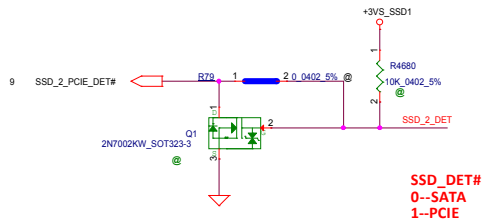



| Security Classification | | | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----------------|------------|
| LC Future Center Secret Data | | | |
| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 |
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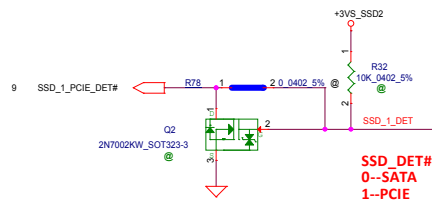
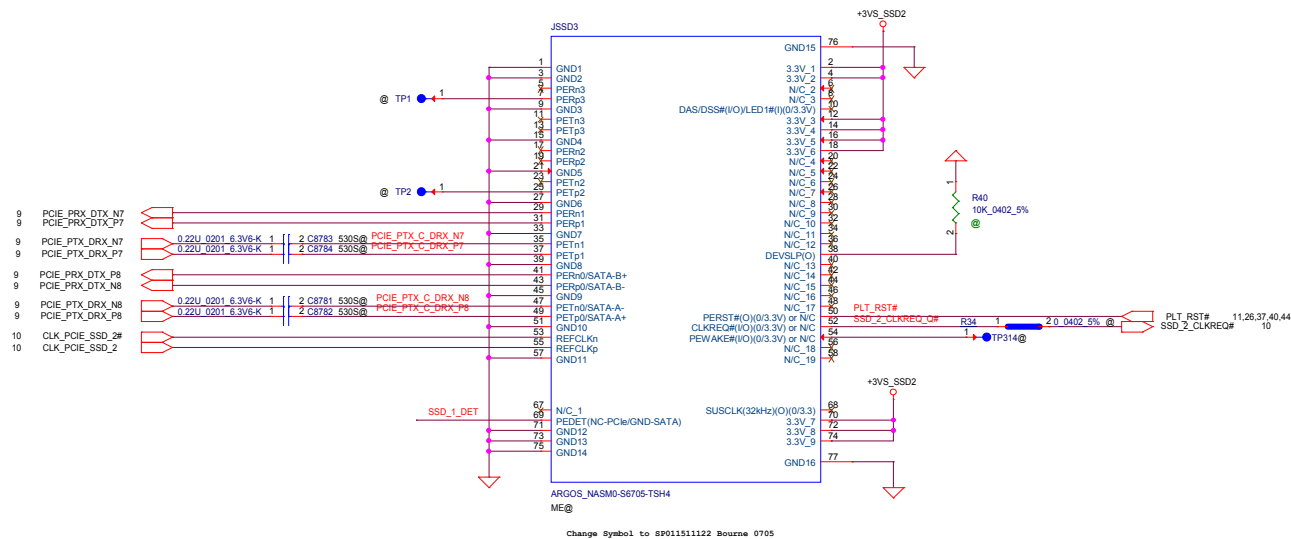
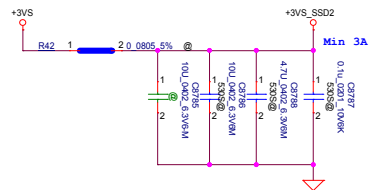
| Title | |
|---------------|---------------------------|
| HALL/G Sensor | |
| Size | Document Number |
| Custom | BYG10 ES430 ES530 |
| Date: | Tuesday, January 05, 2016 |
| Sheet | 36 of 60 |



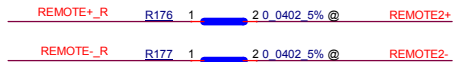
Rev 1.0



| | | | | |
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| Date: Tuesday, January 05, 2016 Sheet: 0 of 3 | | | | |

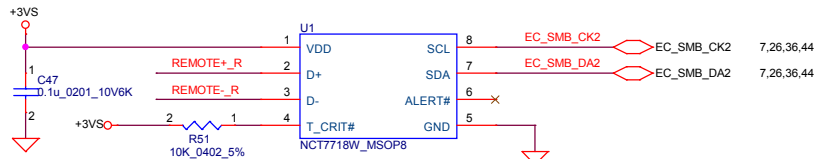


Close to U1



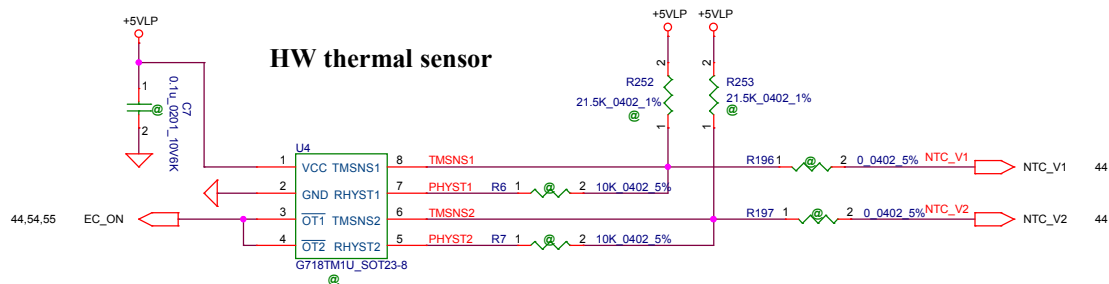
REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

SMSC thermal sensor placed near DIMM



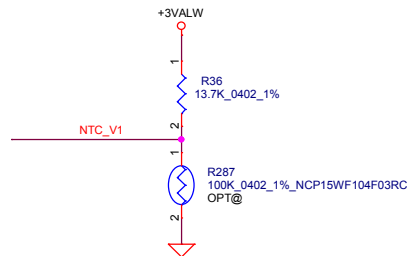
Address 1001_101xb

HW thermal sensor

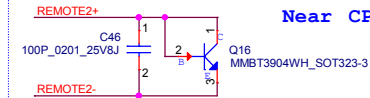


over temperature threshold:
 $RSET = 3 \cdot RTMH$
 $92+/-30C$
Hysteresis temperature threshold.
 $RHYST = (RSET \cdot RTML) / (3 \cdot RTML - RSET)$
 $56+/-30C$

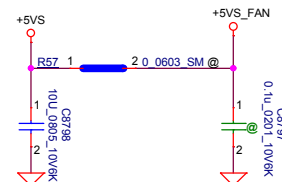
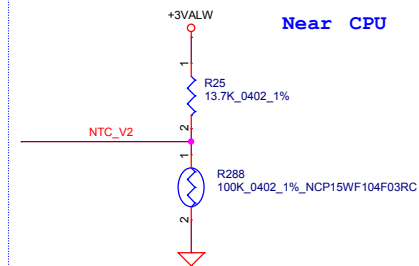
Near GPU&VRAM



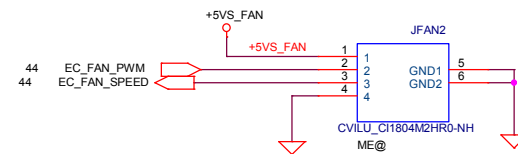
Near CPU core



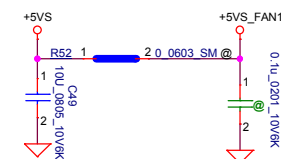
Near CPU



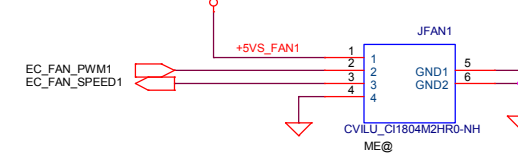
FAN Conn



Change Symbol to SP01001J000 Bourne 0629



FAN Conn

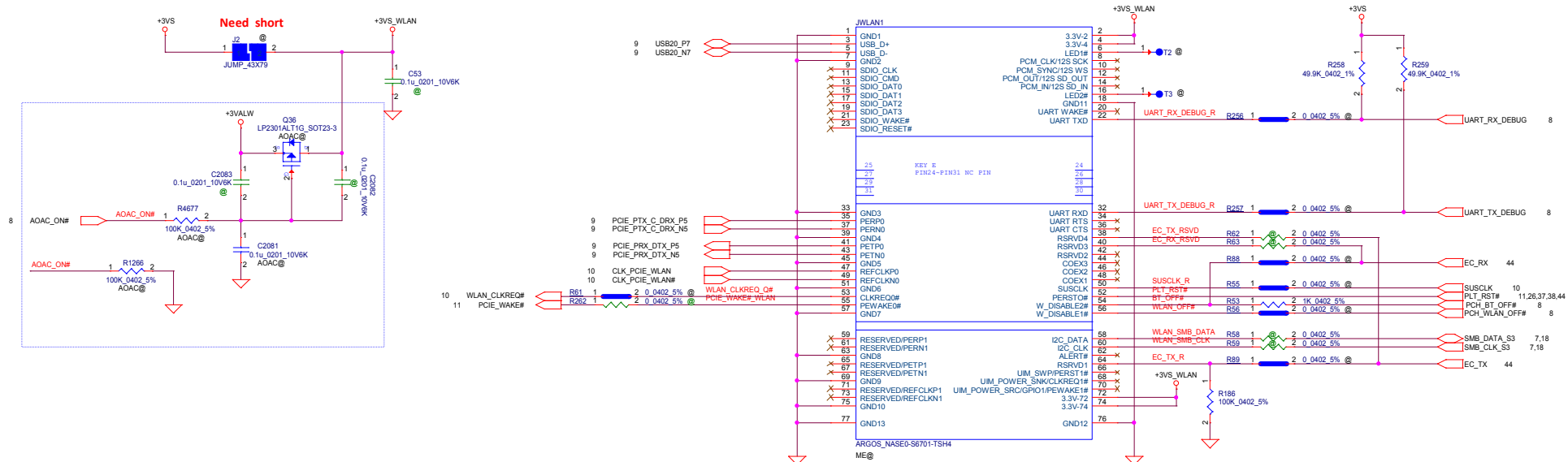


Change Symbol to SP01001J000 Bourne 0629

| Security Classification | | | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----------------|------------|
| LC Future Center Secret Data | | | |
| Issued Date | 2016/08/16 | Deciphered Date | 2017/08/15 |
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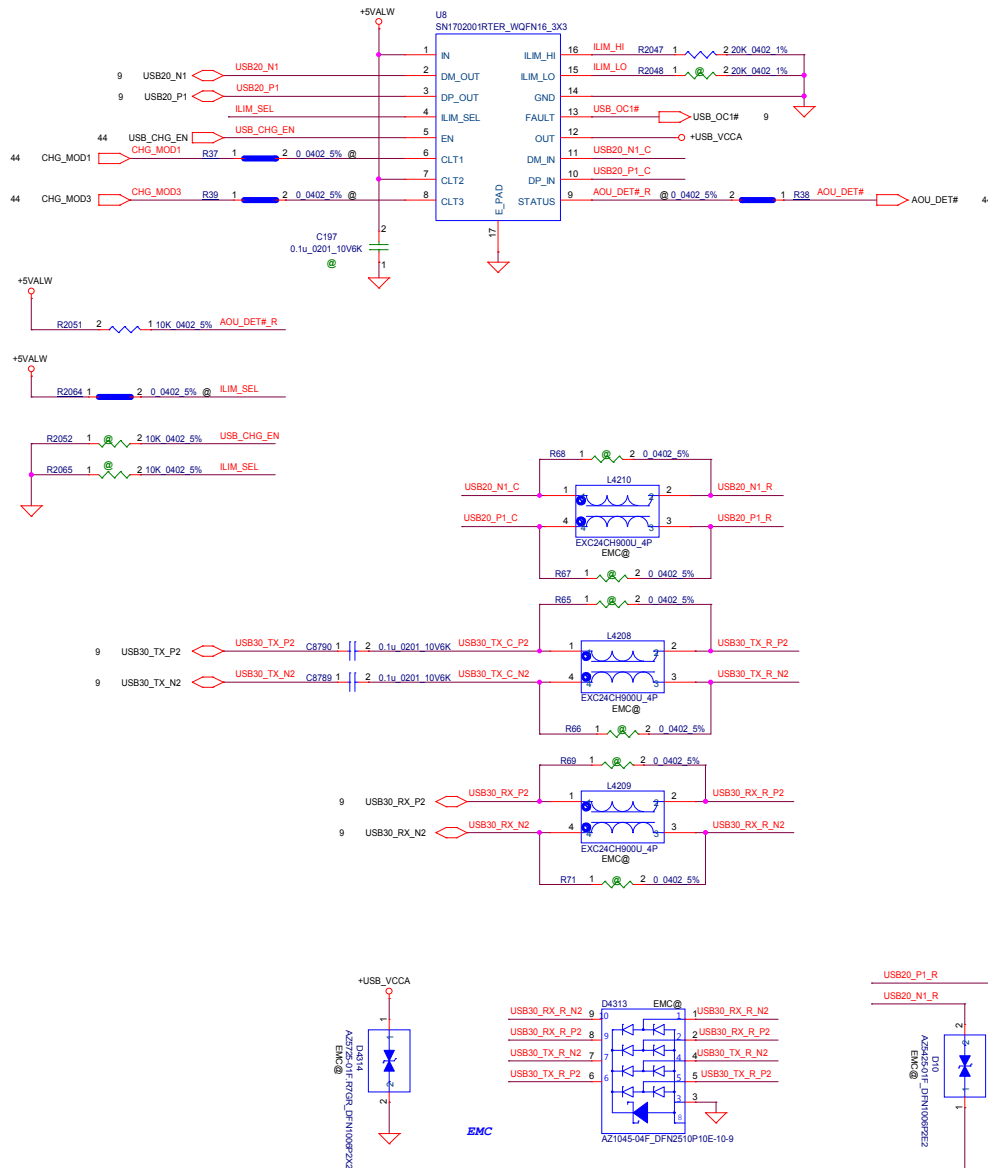
| Title | | | |
|-------------------------|---------------------------|--------|----------|
| Thermal sensor/FAN CONN | | | |
| Size | Document | Number | Rev |
| Custom | Document | Number | 1.0 |
| Date: | Tuesday, January 09, 2018 | Sheet | 39 of 60 |

Mini-Express Card(WLAN/WiMAX)

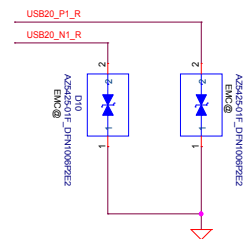
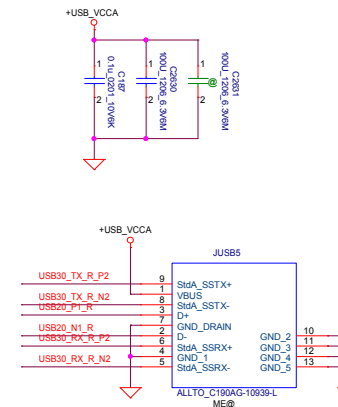



RIGHT SIDE USB3.0 PORT x1

USB charger
2.2A

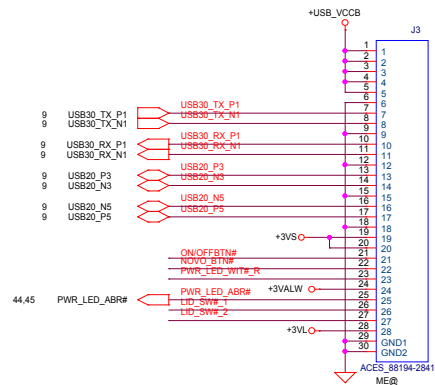
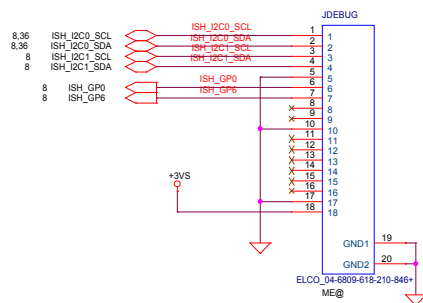
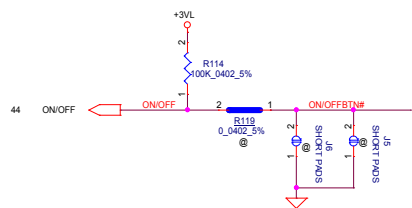
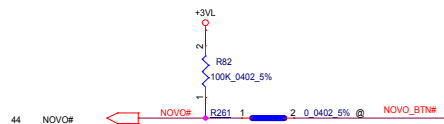
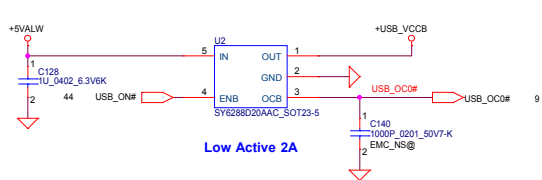



| CLT1 | CLT2 | CLT3 | ILIM_SEL | MOD | |
|------|------|------|----------|-------------|-------------------------------------------------------|
| 0 | 0 | 0 | X | DCH | OUT held low |
| 1 | 1 | 1 | 1 | CDP | Data Connected and Port Power Mgt. Function Active |
| 1 | 1 | 1 | 0 | SDP2 | Data Connected |
| 1 | 1 | 0 | X | SDP1 | Data Connected |
| 0 | 1 | 0 | X | SDP1 | Data Connected |
| 1 | 0 | 0 | X | DCP_Short | Device Forced to stay in DCP BC 1.2 charging mode |
| 1 | 0 | 1 | X | DCP_Divider | Device Forced to stay in DCP Divider 1 Charging Mode |
| 0 | 1 | 1 | X | DCP_Auto | Data Disconnected and Port Power Mgt. Function Active |
| 0 | 0 | 1 | X | DCP_Auto | Data Disconnected and Power Wake Function Active |

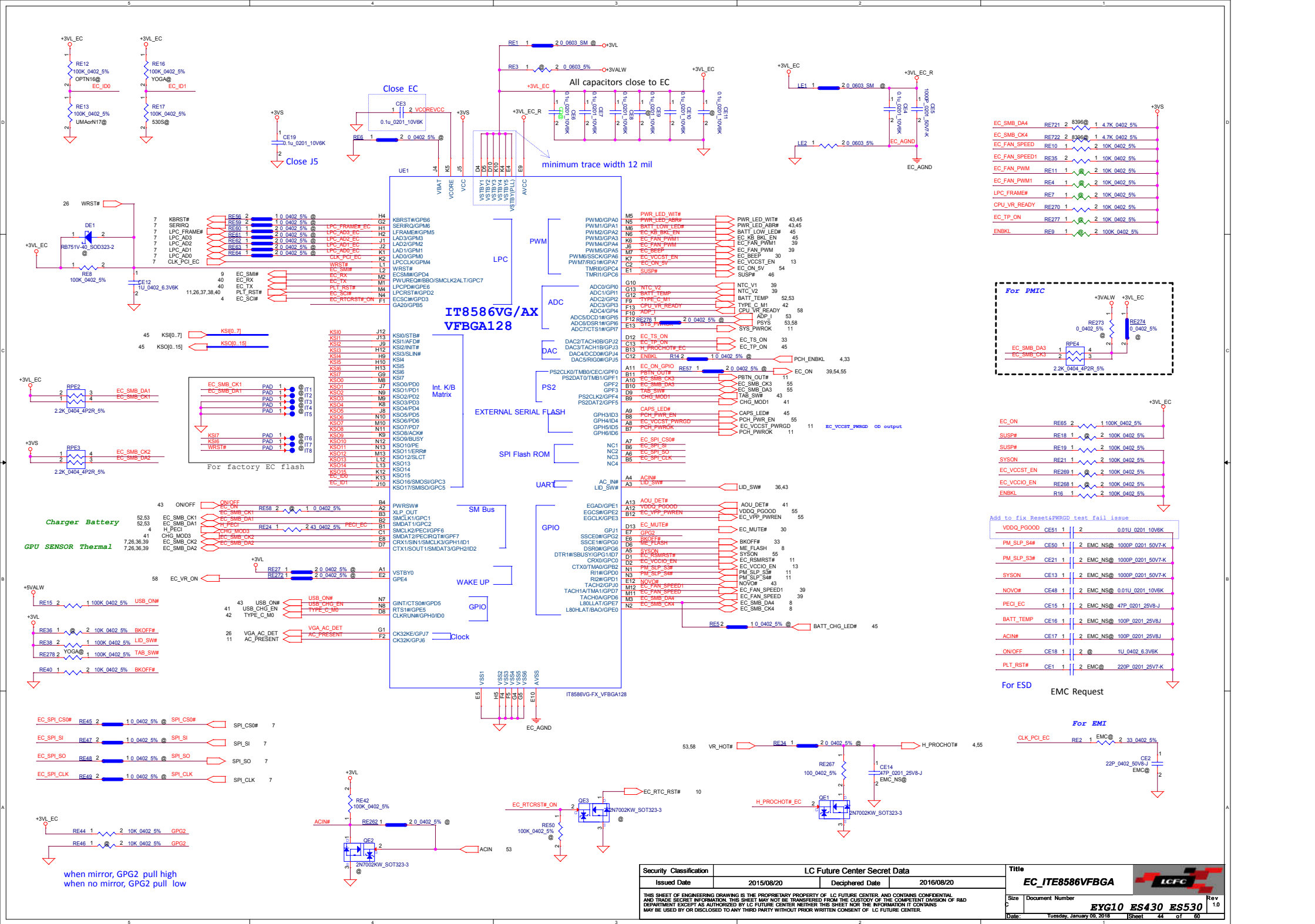


| | | | | | |
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| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | USB3 PORT_LEFT | |
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| | | | | Date: Tuesday, January 09, 2016 Sheet 41 of 60 | Rev 1.0 |

Right SIDE USB3.0 PORT

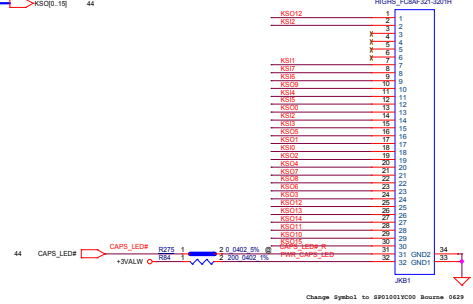
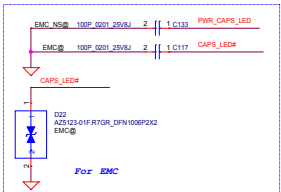


| | | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----------------|------------|--------------------------------------------------|---------------------------------------------------------------------------------------|
| Security Classification | LC Future Center Secret Data | | | Title |  |
| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | I/O_DB_CONN | |
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| | | | | Date: Tuesday, January 09, 2018 | Rev 1.0 |
| | | | | Sheet 43 of 60 | |

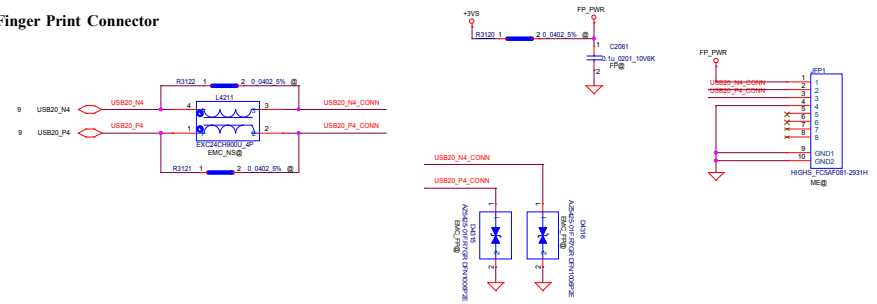


K/B Connector

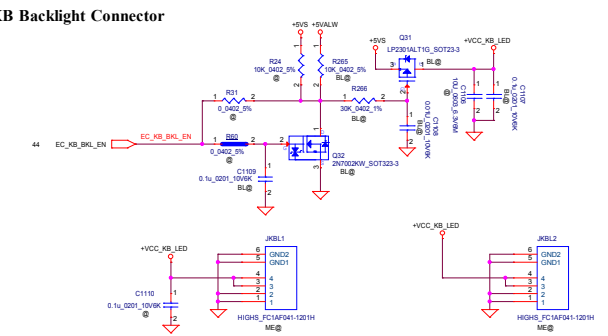
KS00_71 KS00_18



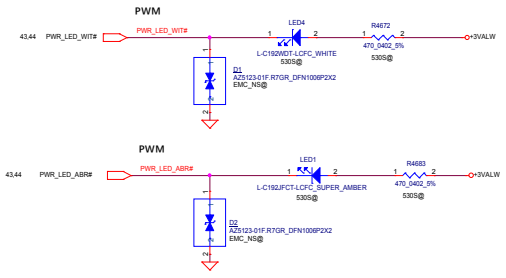
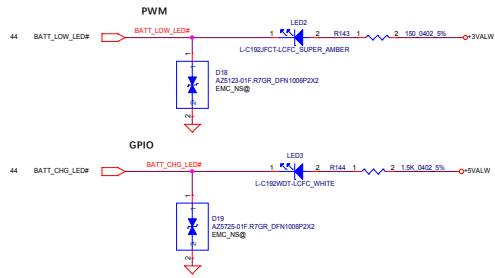
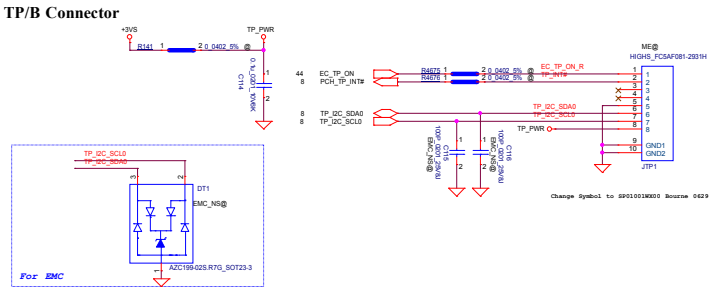
Finger Print Connector



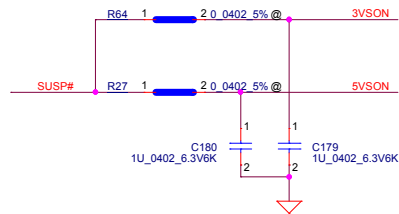
KB Backlight Connector



TP/B Connector

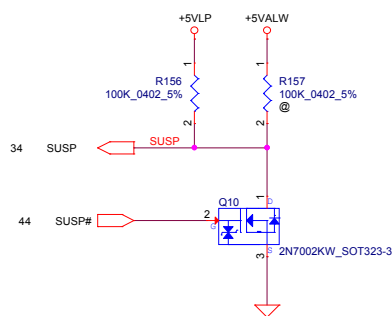
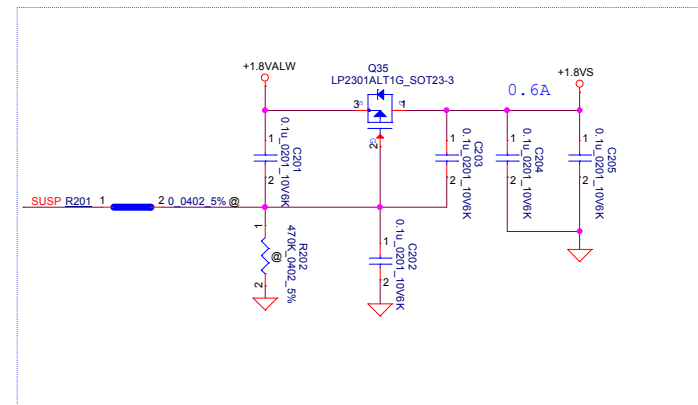
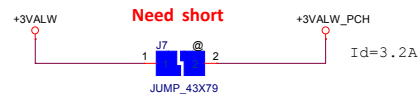
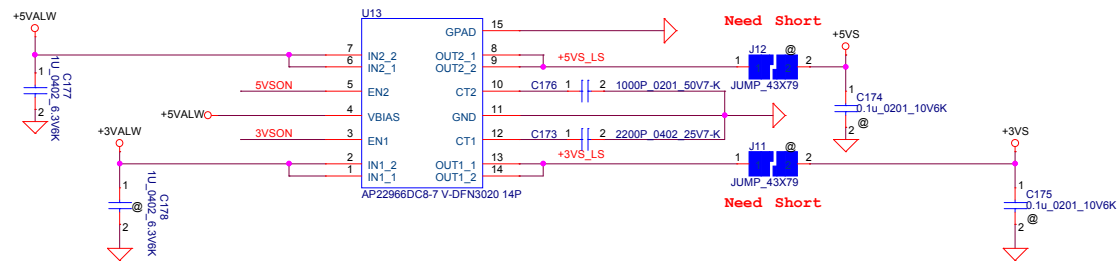


| LED | State | LED Behavior |
|--------------|--------------------|-----------------------------|
| Power Button | System on | White_on (battery#211-100%) |
| | Standby | White_on (battery#211-20%) |
| | Standby LID closed | White_on (battery#211-100%) |
| | System off | White_on (battery#211-20%) |
| Charging | Battery only | off |
| | Charging | White_on (battery#211-100%) |

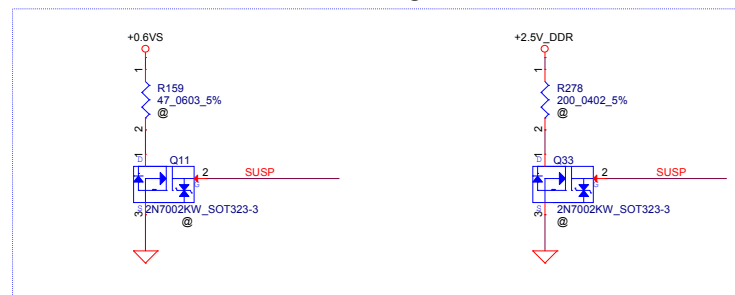


Load Switch
+5VALW To +5VS
+3VALW To +3VS


+3VS, C173 --> 2.74ms
+5VS, C176 --> 2.03ms
VIN 5V and 3.3V (VBIAS=5V), IMAX(per channel)=6A, Rds=16mohm



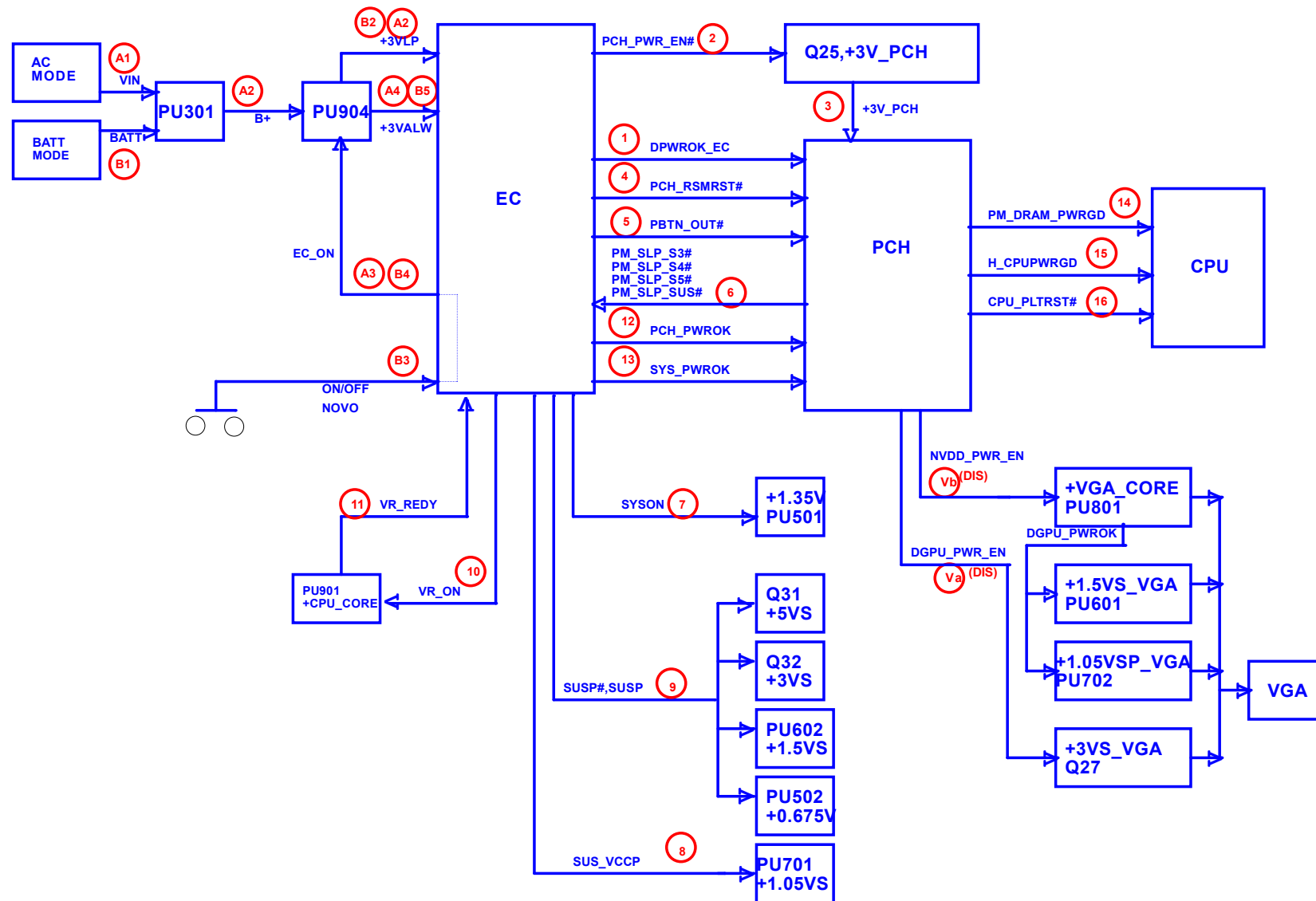
For DisCharge



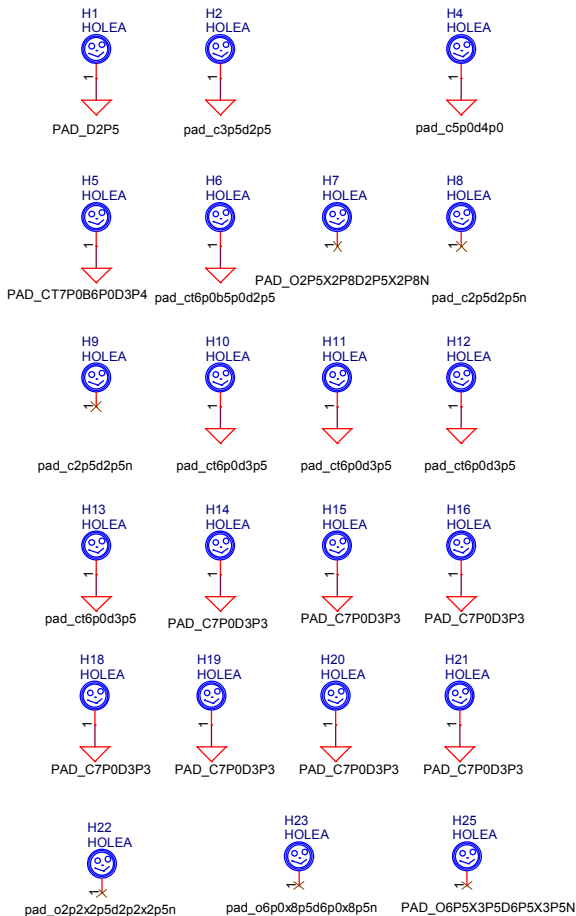
08/29: Need double check enable signal and the resistance

| | | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|------------------------------|------------|---------------------------------------------------------------------------------------|-----------------|
| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | DC V TO VS INTERFACE | |
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| | | | | Size | Document Number |
| | | | | Custom | Revised |
| | | | | Date: | Sheet |
| | | | | | |

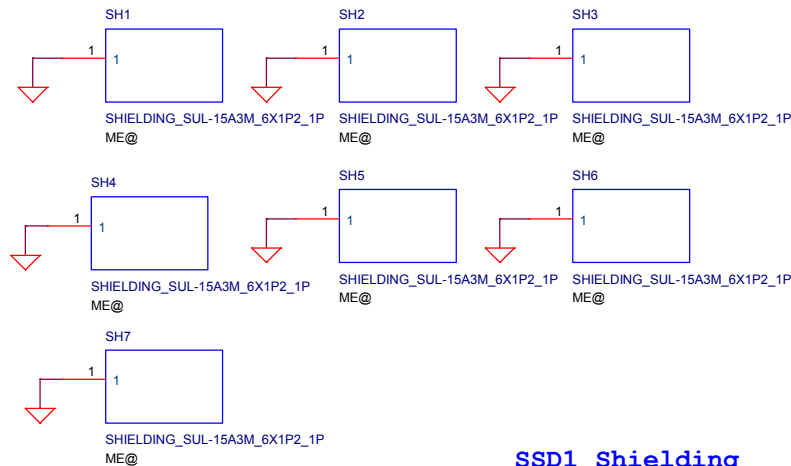
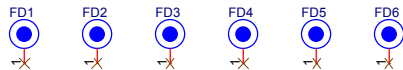
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|---------------------------|----------|---------|
| EYG10 ES430 ES530 | | Rev 1.0 |
| Tuesday, January 09, 2018 | 46 of 60 | |



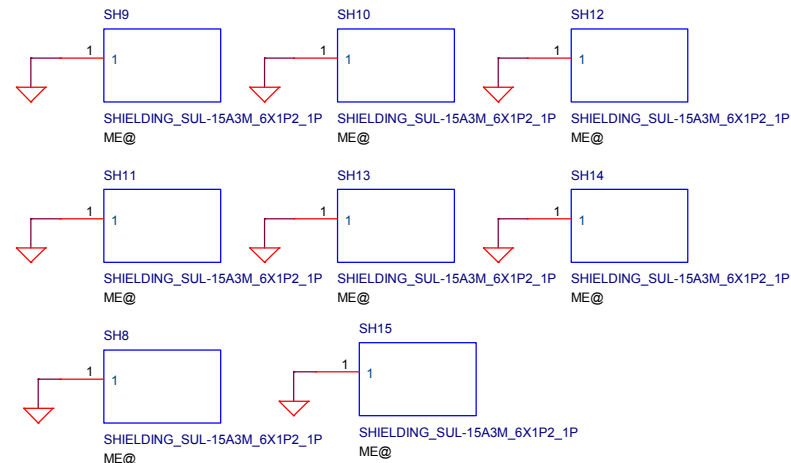
Hole




PCB Federal Mark PAD



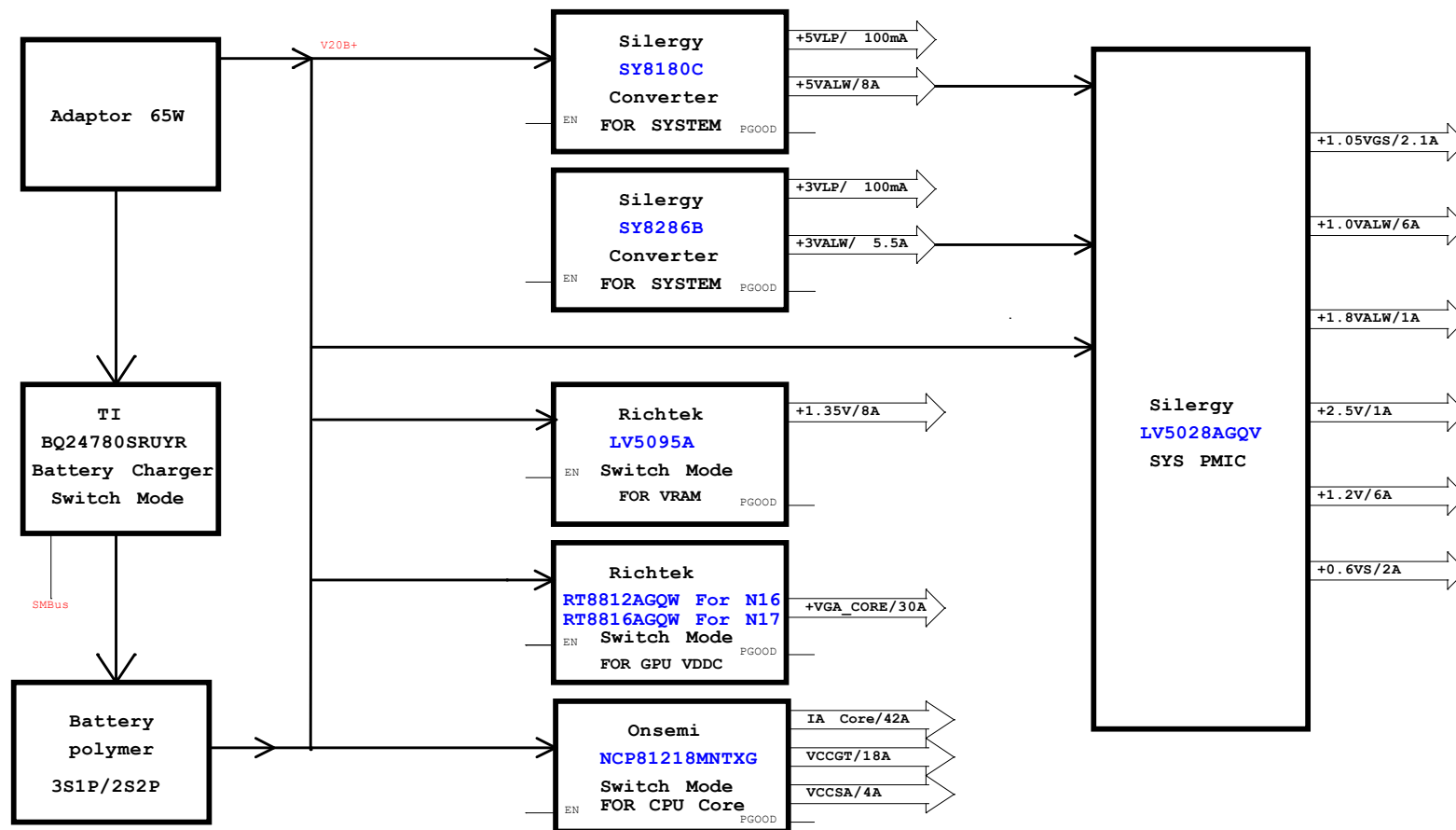
SSD1 Shielding

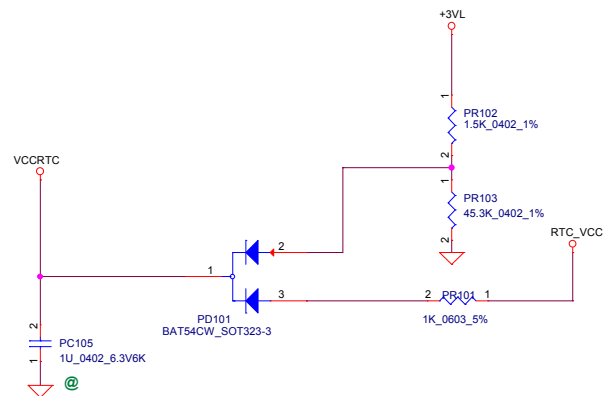



DDR Shielding

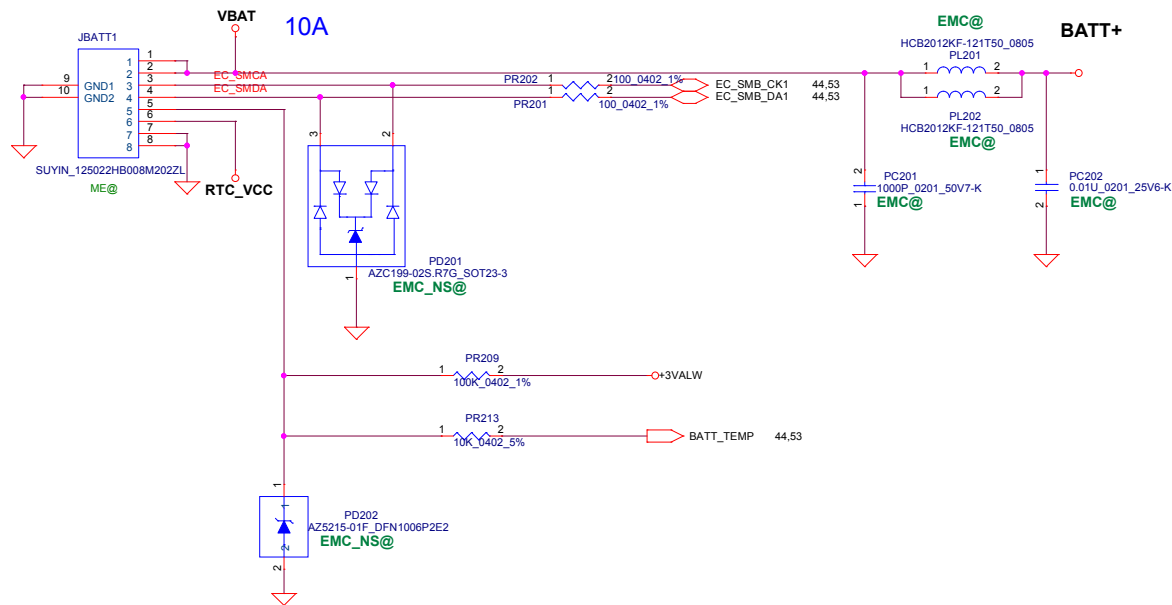
| | | | | | | |
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| Security Classification | | LC Future Center Secret Data | | Title | |  |
| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | Hole | | |
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| | | | | Date: | Tuesday, January 09, 2018 | Sheet 49 of 60 |
| | | | | | BYG10 ES430 ES530 | 1.0 |

EYG10 ES430 ES530

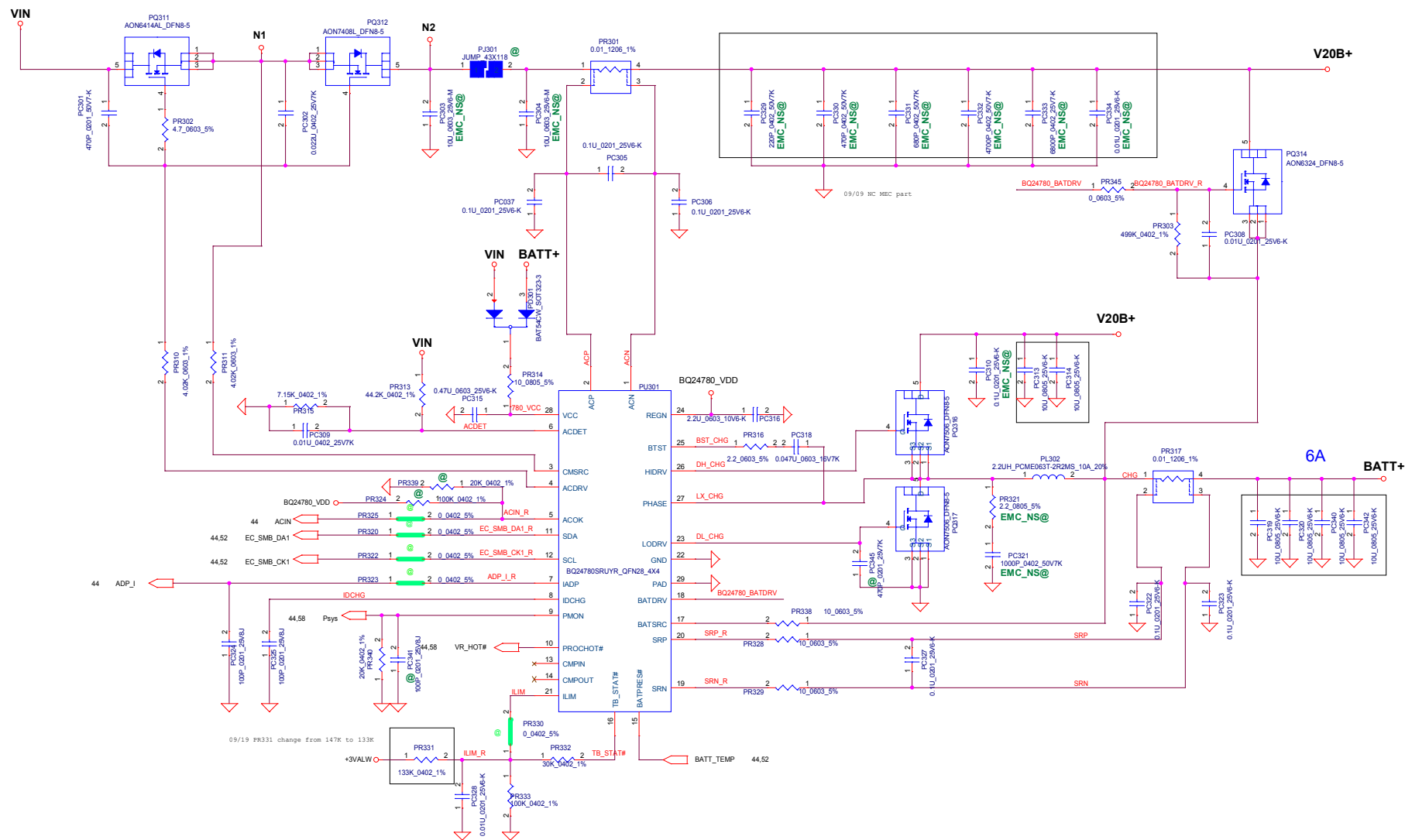




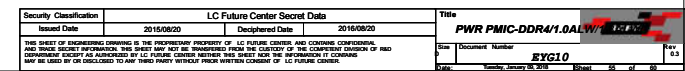
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| Security Classification | | LC Future Center Secret Data | | Title | |
| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | PWR-DCIN / RTC charger  | |
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| | | | | Date: | Tuesday, January 06, 2018 Sheet 51 of 60 Rev 0.5 |



2S1P polymer battery
voltage level: +5.5V ~
8.8 V



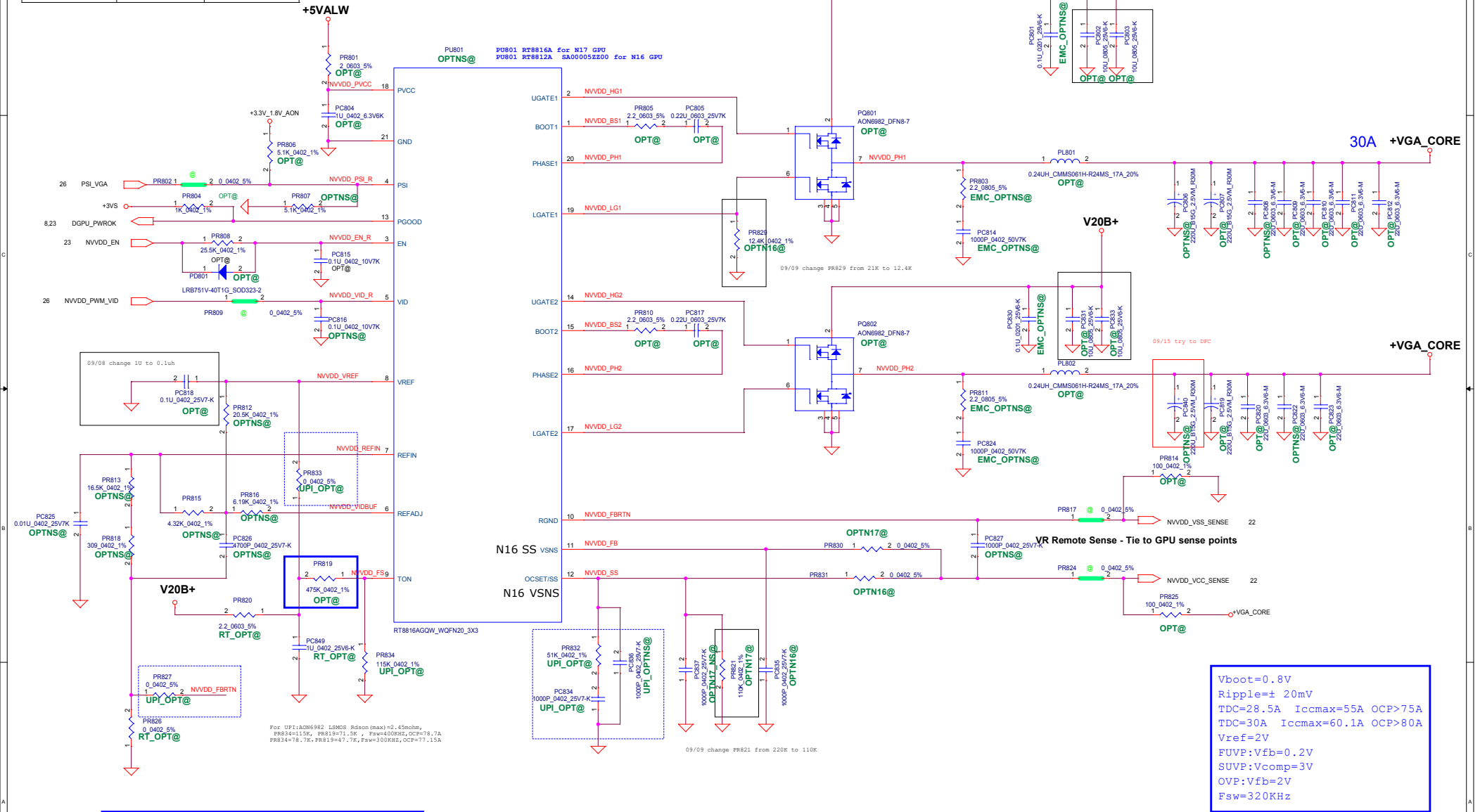
ACDECT setting 17.2V
 Charge current limit HW=7A
 DC discharge limit =26A
 Discharge current limit HW=9A during Turbo boost



| PWM-VID Specification | | | |
|-----------------------|------------|------------|---|
| | N17 Config | N16 Config | B |
| Vmin(V) | 0.3 | 0.6 | |
| Vmax(V) | 1.3 | 1.2 | |
| Vboot(V) | 0.8 | 0.9 | |
| Vstep(mV) | 6.25 | 6.25 | |
| N(level) | 160 | 96 | |
| Fpwm(KHz) | 675 | 1.125 | |
| Tdmin(nS) | 9.26 | 9.26 | |
| T(uS) | <100 | <100 | |

| Component | Value | N17 | N16S-GTR |
|-----------------|-------|-------|----------|
| R1(K Ω) | PR816 | 6.19 | 20 |
| R2(K Ω) | PR812 | 20.5 | 20 |
| R3(K Ω) | PR815 | 4.32 | 2 |
| R4(K Ω) | PR813 | 16.5 | 18 |
| R5(K Ω) | PR818 | 0.309 | 0 |
| C(nF) | PC826 | 4.7 | 2.7 |

| RT8816 PSI | RT8812 PSI | Phase Configuration |
|------------|------------|---------------------|
| 1.6V~5.5V | 2.4~5.5V | 2Phase CCM |
| 1.08~1.35V | | 2Phase DEM |
| 0.7~0.88V | 1.2~1.8V | 1Phase CCM |
| 0~0.4V | 0~0.8V | 1Phase DEM |

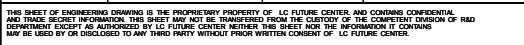


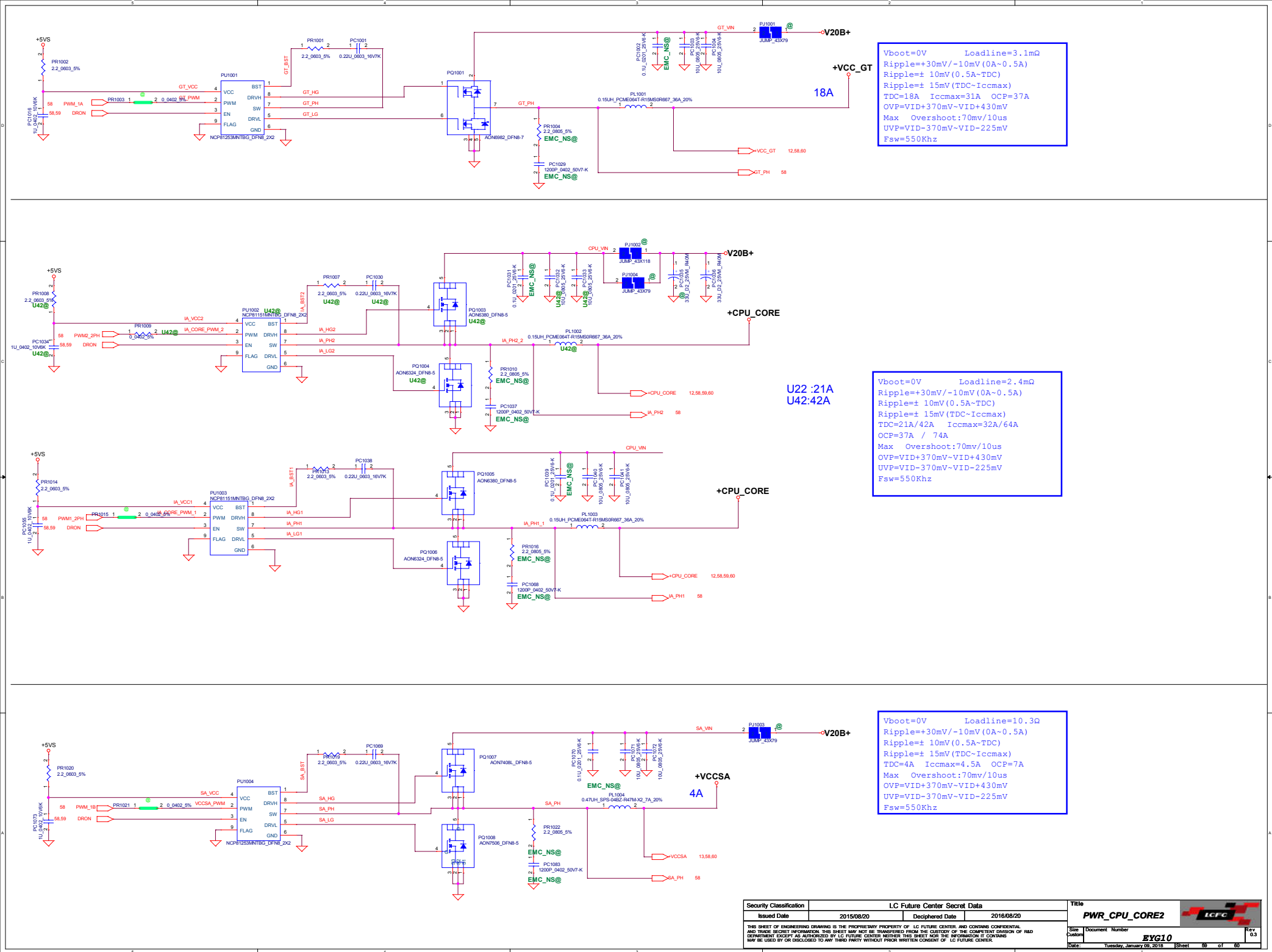
| Security Classification | LC Future Center Secret Data | |
|-------------------------|------------------------------|-----------------|
| Issued Date | 2015/08/20 | Deciphered Date |
| | | 2016/08/20 |

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| Title | | PWR-VGA_CORE | |
|-------|---------------------------|--------------|----------|
| Size | Document Number | EYG10 | |
| Date: | Tuesday, January 05, 2016 | Sheet | 57 of 60 |

| | | | |
|--------|------|----|-------|
| RVboot | Core | GT | SA |
| 35.7K | 0V | 0V | 1.05V |





1106 NC PC4028,PC4010
0915 NC PC4008,PC4025,PC4026,
0915 NC PC4007,PC4027


[illegible]

CPU CORE U42 only: 5PCS 22U 0402 4V

09/09 NC PC4070,PC4068 10UF,mount PC4035,PC4037 10uf

```
09/09 PC4086 from U42 22uf to U42 22uf/u22 10uf
PC4080 from U42 10uf to U42 22uf/U22 10uf
PC4038 from U22 22uf to U22 22uf/U42 10uf
```

+VCCSA

| | | | | | |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------|-----------------|------------|-------------------------------|---------------------------------------------------------------------------------------|
| Security Classification | LC Future Center Secret Data | | | Title |  |
| Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | PWR-CPU Decoupling Cap | |
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| Size Custom | Document Number | | | EYG10 | Rev |
| Date: | Tuesday, January 05, 2018 | | | Sheet | 60 of 1 |

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| <table><tr><td colspan="2">Security Classification</td><td colspan="2">LC Future Center Secret Data</td><td>Title</td></tr><tr><td>Issued Date</td><td>2015/08/20</td><td>Deciphered Date</td><td>2016/08/20</td><td>NGFF_SSD_1</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER.</td><td><table><tr><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td>C</td><td>EYG10</td><td>0.3</td></tr><tr><td>Date:</td><td>Tuesday, January 09, 2018</td><td>Sheet 61 of 60</td></tr></table></td></tr></table> | | | | | Security Classification | | LC Future Center Secret Data | | Title | Issued Date | 2015/08/20 | Deciphered Date | 2016/08/20 | NGFF_SSD_1 | THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF LC FUTURE CENTER, AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY LC FUTURE CENTER. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF LC FUTURE CENTER. | | | | <table><tr><td>Size</td><td>Document Number</td><td>Rev</td></tr><tr><td>C</td><td>EYG10</td><td>0.3</td></tr><tr><td>Date:</td><td>Tuesday, January 09, 2018</td><td>Sheet 61 of 60</td></tr></table> | Size | Document Number | Rev | C | EYG10 | 0.3 | Date: | Tuesday, January 09, 2018 | Sheet 61 of 60 |
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| Date: | Tuesday, January 09, 2018 | Sheet 61 of 60 | | | | | | | | | | | | | | | | | | | | | | | | | | |
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